

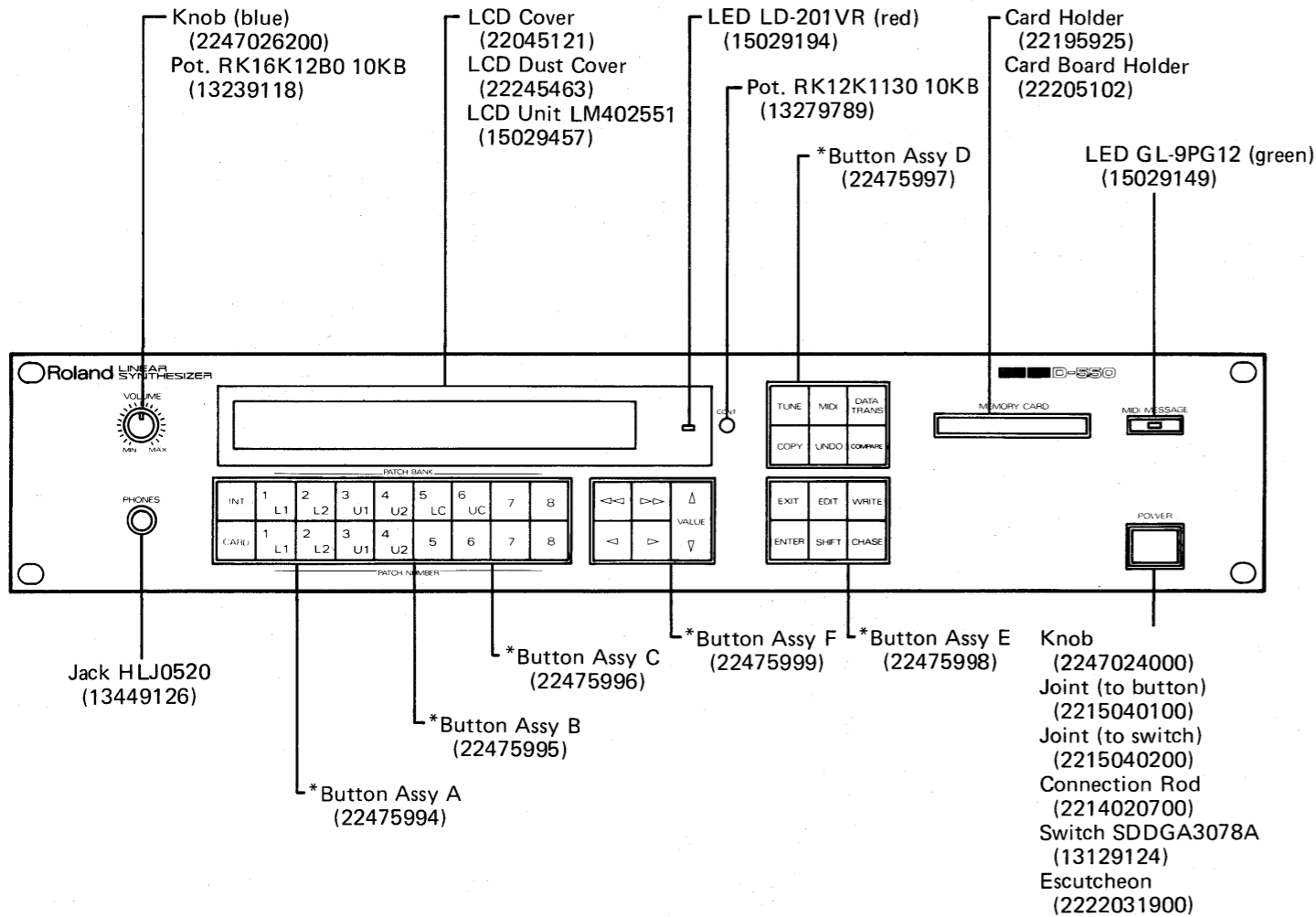
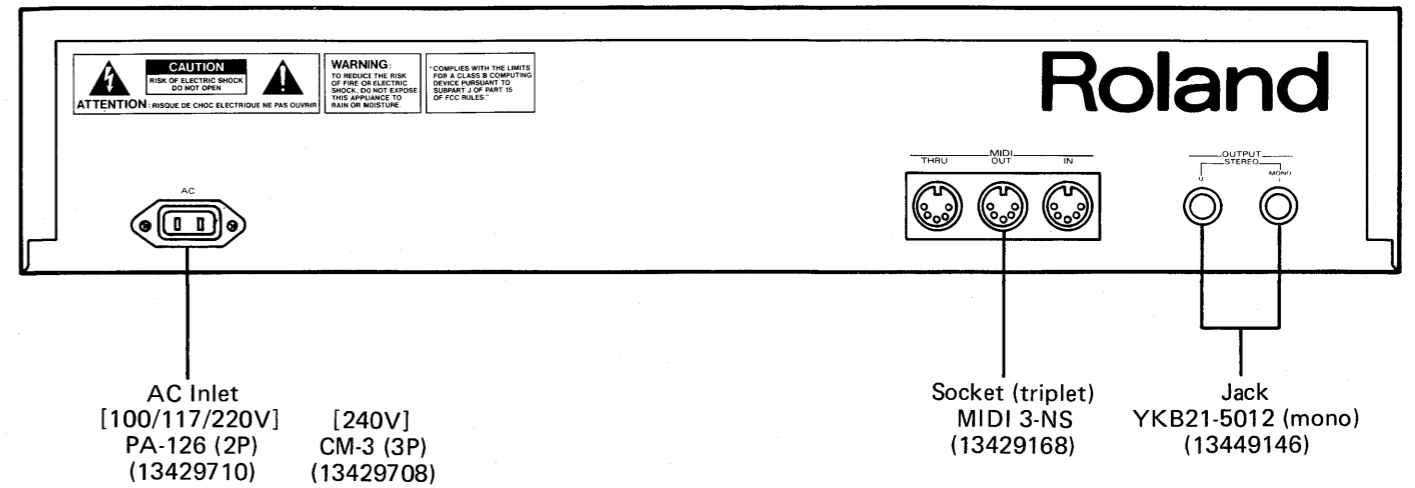
D-550

SERVICE NOTES

First Edition

SPECIFICATIONS

TUNE	MASTER TUNE	±50 cents	CHORUS LFO	RATE	0.098 – 20Hz
	FINE TUNE	±50 cents	OUTPUT	AUDIO	–4.0dBm
PITCH MODULATION	LFO	±600 cents		PHONES	8 – 150Ω Stereo
	ENV	±2400 cents	POWER CONSUMPTION15W, 12W (Japan)	
	BENDER	±2400 cents	DIMENSIONS483(W) x 414(D) x 90(H) mm	
ENV TIME	AFTERTOUC	±2400 cents		18-7/8" x 16-1/8" x 3-7/16"	
	PITCH T1 – T4	9ms – 9s	WEIGHT6.3 kg/14 lb 6 oz	
	TVF T1 – T5	4ms – 80s	ACCESSORYMEMORY CARD (ROM) PN-D50-00	(12379401)
	TVA T1 – T5	4ms – 80s			
LFO	RATE	0.0004 – 27Hz			
	DELAY TIME	0 – 10s			



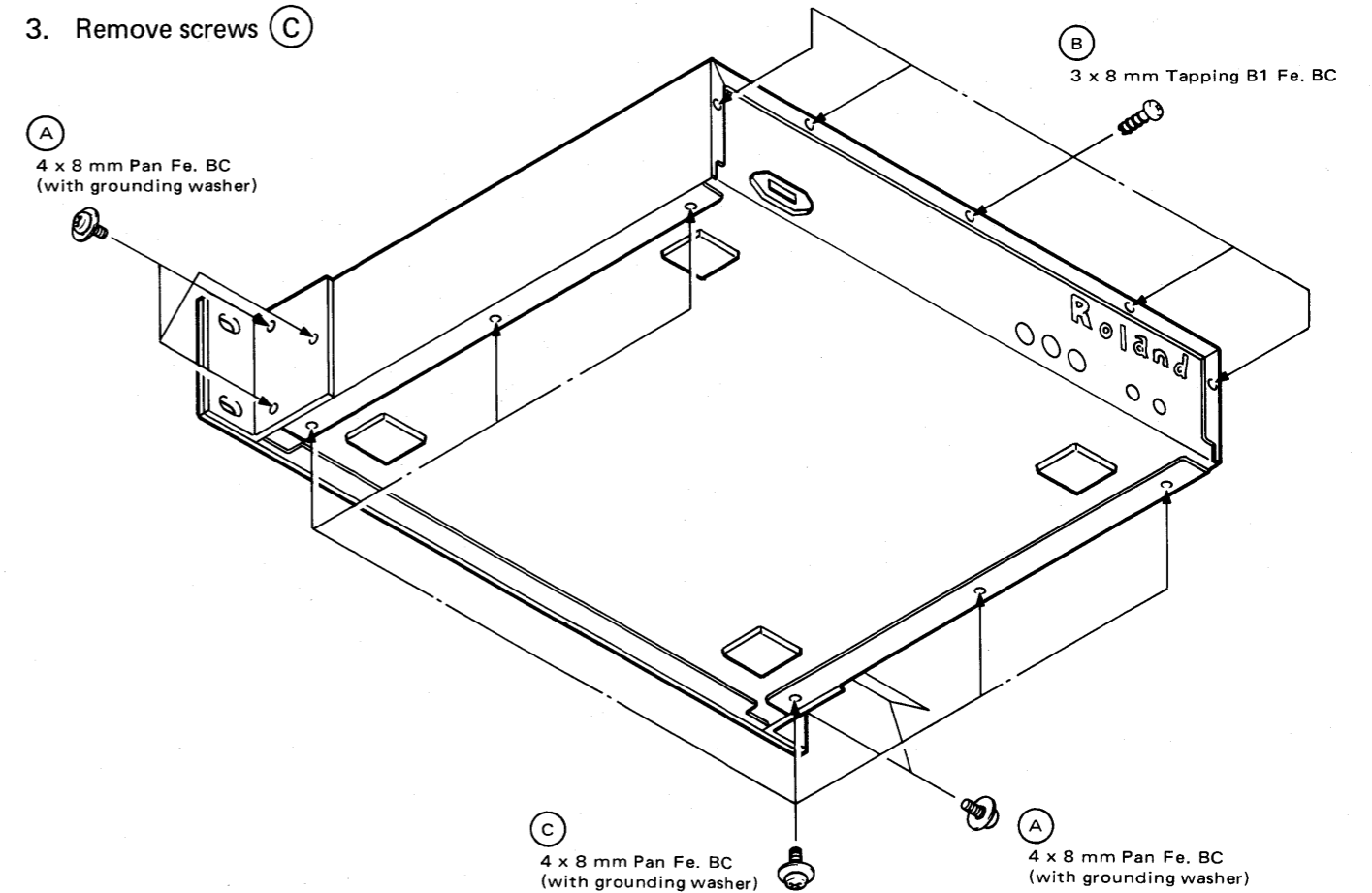
*Switch SKHHBS (13129733)

*The part No. of each button is as listed below. (Button Frame (3P) of each Button Assy: Part No. 2247024000)

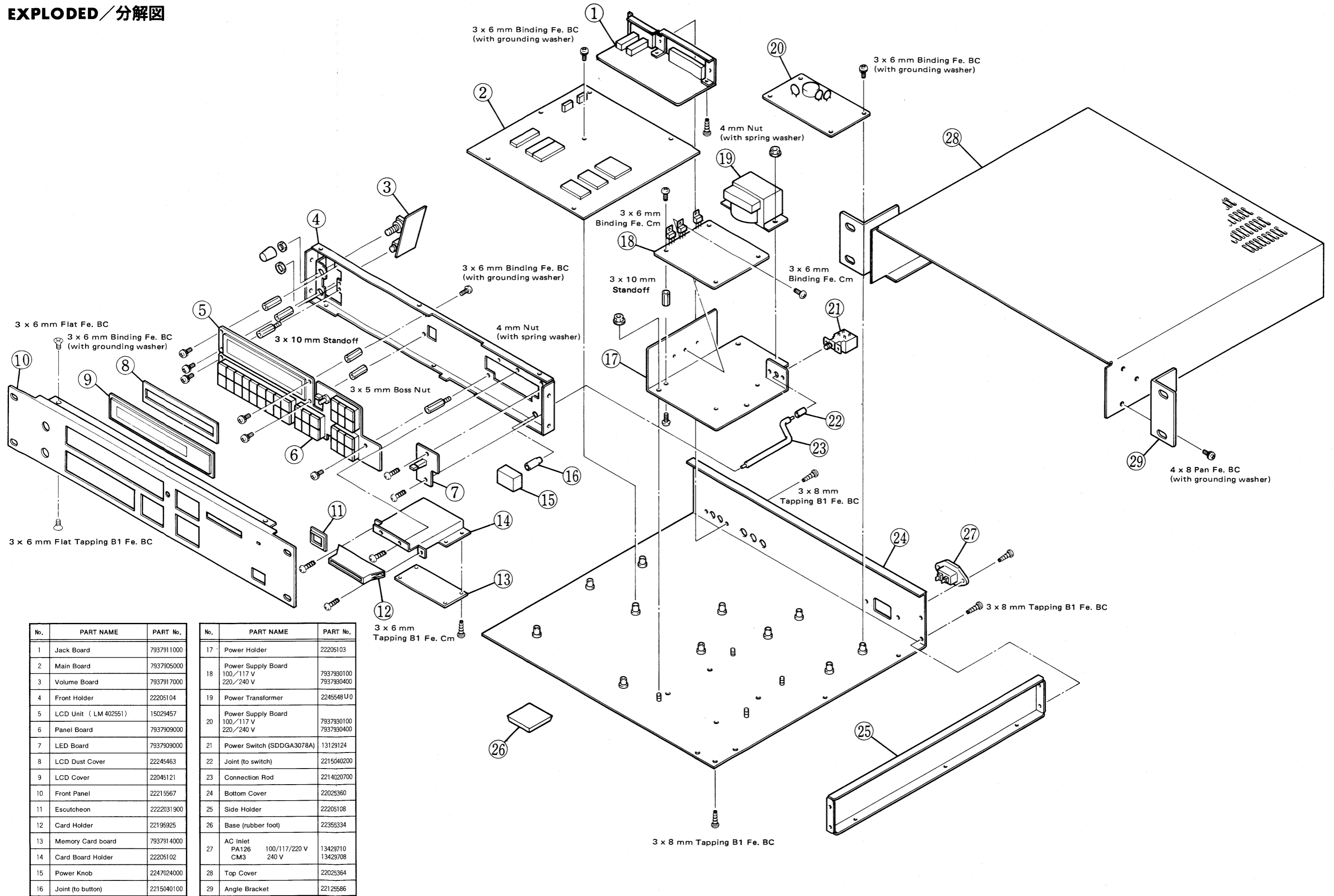
22495562	INT	22495557	5	22495551	←	22495546	ENTER	22495540	COMPARE
22495561	CARD	22495556	5 LC	22495550	△	22495545	CHASE	22495539	UNDO
22495563	1 L1	22495555	6	22495549	▷▷	22495544	SHIFT	22495538	COPY
22495560	2 L2	22495554	6 UC	22495548	▷	22495543	WRITE	22495537	DATA TRANS
22495559	3 U1	22495553	7	22495547	VALUE	22495542	EDIT	22495536	MIDI
22495558	4 U2	22495552	8			22495541	EXIT	22495535	TUNE

DISASSEMBLING / 分解手順

1. Remove screws (A)
2. Remove screws (B)
3. Remove screws (C)



EXPLODED / 分解图



No.	PART NAME	PART No.
1	Jack Board	7937911000
2	Main Board	7937905000
3	Volume Board	7937917000
4	Front Holder	22205104
5	LCD Unit (LM 402551)	15029457
6	Panel Board	7937909000
7	LED Board	7937909000
8	LCD Dust Cover	22245463
9	LCD Cover	22045121
10	Front Panel	22215567
11	Escutcheon	2222031900
12	Card Holder	22195925
13	Memory Card board	7937914000
14	Card Board Holder	22205102
15	Power Knob	2247024000
16	Joint (to button)	2215040100

No.	PART NAME	PART No.
17	Power Holder	22205103
18	Power Supply Board 100/117 V 220/240 V	7937930100 7937930400
19	Power Transformer	2245548U0
20	Power Supply Board 100/117 V 220/240 V	7937930100 7937930400
21	Power Switch (SDDGA3078A)	13129124
22	Joint (to switch)	2215040200
23	Connection Rod	2214020700
24	Bottom Cover	22025360
25	Side Holder	22205108
26	Base (rubber foot)	22355334
27	AC Inlet PA126 100/117/220 V CM3 240 V	13429710 13429708
28	Top Cover	22025364
29	Angle Bracket	22125586

PARTS LIST

Since most of chip components on the main board can be replaced by locally available ones, this list represents special ones only.

メイン・ボード上のチップ部品は交換可能です。交換の際は、特殊なチップ部品を除き通常のパーツで代用してください。(パーツ・リストには、代用できないチップ部品のみ記載しています。)

CASING

22215567	Front Panel
22025364	Top Cover
22025360	Bottom Cover
22205104	Front Holder
22205108	Side Holder
22125586	Angle Bracket
22045121	LCD Cover
22195889	MIDI Holder
22205101	Jack Holder
22195925	Card Holder
22205102	Card Board Holder
22205109	Headphone Holder
22205103	Power Holder
2222031900	Escutcheon
22355334	Base (Rubber Foot)

BUTTON/KNOB

*For each button see the front Page.

それぞれのボタンについては表紙を見て下さい。

22475994	Button Assy A	INT, CARD, PATCH BANK 1/2, PATCH NUMBER 1/2
22475995	Button Assy B	PATCH BAND 3/4/5, PATCH NUMBER 3/4/5
22475996	Button Assy C	PATCH BANK 6/7/8, PATCH NUMBER 6/7/8
22475997	Button Assy D	TUNE, COPY, MIDI, UNDO, DATA TRANSFER, COMPARE
22475998	Button Assy E	EXIT, EDIT, SHIFT, ENTER, WRITE, CHASE
22475999	Button Assy F	<<, >>, >, <, VALUE
2247026200	Knob blue	VOLUME
2247024000	Knob	POWER
2247024000	Button Frame (3P)	

AC CORD SET (detachable)

13439825	DC-320J01	100V
13439812F0	UC-704J01	117V
13439813F	EC-210J06	220V
23495110	BB6742-BB6791	240V England
13439814F0	SC-415J06	240V Australian

SOCKET

13429710	PA-126 2P AC Inlet	100/117/220V
13429708	CM-3 AC Inlet	240V
13429168	MIDI 3-NS (triplet)	MIDI IN/OUT/THRU
13449146	YKB21-5012 (mono)	OUTPUT (U/L)
13449126	HLJ0520	PHONES
13429534	ICE-286-S-TG	EP ROM

SWITCH

13129733	SKHHBS	panel board
13129124	SDDGA3078A	power switch

FUSE

12559411	SD6 315MA	100/117V
12559380	SD6 1.25A-N1	100/117V
12559540	CEE-160MAT BESWICK	220/240V
12559549	CEE-1.25AT BESWICK	220/240V

POWER TRANSFORMER

22455480U0	Power (universal)	100/117/220/240V
12449567	NEL D32-43 (EL inverter)	power supply board

LCD UNIT

15029457	LM402551 with EL, PCB and wiring
*No replacement for individual parts.	
補修品はユニット単位	

PCB ASSEMBLY

7937905000	Main Board (PCB 22925445)
7937911000	Jack Board (PCB 22925491)
7937914000	Memory Card Board (PCB 22925491)
7937909000	Panel/LED Board (PCB 22925491)

*Panel board and LED board are supplied together in a set.

パネル・ボードとLEDボードは、セットで供給します。

7937917000	Volume Board (PCB 2295491)
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7937930100	Power Supply Board 100/117V (PCB 22925490)
7937930400	Power Supply Board 220/240V (PCB 22925490)

*The same Assy number is applied to both primary and secondary boards. Specify which of them is required, when ordering.

一次側と二次側のボードは同じアッセンブリ・ナンバーになっています。

発注の際は、いずれのボードかを明記して下さい。

POTENTIOMETER

13239118	RK16K12B0	10kΩ	VOLUME
13279789	RK12K1130	10kΩ	CONTRAST
(trimmer)			
13299197	EVN-D4AA00B15		D/A

INDUCTOR

12449294	BL03RN2-R62T2		main board, jack board, volume board
12449291	BL02RN1-R62		power supply board
12449265	ELE-H102KA	1mH	power supply board
12449301	SN3-300	20μH	main board

FILTER

22445293	TFB-3 fc=14.5kHz	LC filter
13529149	ELXTV103EA	digital noise filter
13529150	DSS310-55B101M	EMI filter
12449298	ESD-R-25D	data line filter
		(line on Volume board)
12449229	FK0B-160MH15	power supply board

OPT-ISOLATOR

15229718	6N137
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CRYSTAL

12389774	HC49/U10	32.768MHz	synthe chip
12289765	TQC-226A-6R	12MHz	CPU

RESISTOR ARRAY

13919185	RKM6L103F	10k x 6
(chip)		
15399910	MNRDM8-JX682E	6.8 x 8
15399908	MNRDM2-JX153E	15k x 2
15399907	MNRDM4-JX153E	15k x 4
15399906	MNRDM8-JX153E	15k x 8

CAPACITOR

13529132	RPE132-901F104Z25	0.1μF/25V	ceramic
13659216M0	ECESIEU682K	6800μF	power supply board
13639194S0	35MV1000H	1000μF/25V	power supply board
13529148	DSR1100-56E222MVA2EA		power supply board
13529104	DE7150F472MVA1	4700pF	power supply board

IC

(main board)		
15179266	μPD78312G-022	CPU
15229851	MB87136	synthe chip
15229842	MB87137	chorus chip
15229866	MB87126-006	reverb chip
15229849	HG61H25B18F	gate array
15229848	μPD6500G-062	gate array
15179835	TC532000P-7469	PCM ROM (A)
15179836	TC532000P-7470	PCM ROM (B)
15449111	MBM27C512	EP ROM

*When ordering EP ROM, specify version number.

EP ROM を発注される場合は、バージョン・ナンバーを明記してください。

15179369	HM6264ASP	S RAM
15179374H0	HM62256LP	S RAM
15179376	MB81416-10	D RAM
(15179380)	μPD41416	D RAM D-50)

*Although MB81416-10 and μPD41416 (for D-50) are interchangeable, mix use of different types on the same PCB will lead to unreliable operation.

D-50 の DRAM と互換性はありますが、異なった種類を混ぜて使用しないで下さい。

15219162	PCM54	D/A Converter
15259701T0	TC74HC00F-T2	quad 2-input NAND gate
15259709T0	TC74HC10F-T2	triple 3-input NAND gate
15259740T0	TC74HC139F-T2	dual 2-to-4 line decoder
15259757T0	TC74HC174F-T2	hex D-type flip flop with clear
15259102	μPD4066BG	quad bilateral switch
15289106	M5238FP	low noise OP amp (dual in line)
15289105	μPD4570G	low noise OP amp (dual in line)
15289110	μPC4062G	J-FET-OP amp (dual in line)

(jack board)		
15189190	M5216L	OP amp (dual in line)
15189189	μPC4570HA	low noise OP amp (dual in line)
15169304H0	HD74LS04P	hex inverters

(power supply board)		
15199156	M5F78M12	voltage regulator
15199157	M5F79M12	voltage regulator
15199155	L78MR05R	voltage regulator

TRANSISTOR

15129182	2SC3327A	jack board
15119132	2SA1015GR	jack board
15129176	2SC945AQ-T	power supply board

(chip)		
15309101	2SA1037K	main board
15329502	DTC 124EK	main board
	with built-in resistors	

DIODE

15019126D0	ISS-133		panel board, jack board
150196120X	0.5-5.1X 5.1V zener		power board
15019281	1SR35-100A T-93 100V 1A		power board
15019245SN	S1VB10 100V 1A rectifier		power board
15019272	2B4B41 100V 2A bridge rectifier		power board
(chip)			
15339103	MA153		main board
15339105	DAN202K		main board
(LED)			
15029149	GL-9PG12	green	MIDI MESSAGE
15029152	GL-9HD12	red	CHASE
15029194	LD-201VR	red	MONO MODE

CONNECTOR

(straight type)			
13439260	5267-03A	3P	wafer assy
13439263	5267-06A	6P	wafer assy
13439264	5267-07A	7P	wafer assy
13436326	5219-02A	2P	power board
13439306	5566-06A	6P	power board
(straight type)			
13439330	IL-S-3P-S2T2-EF	3P	connector pin header
13439320	IL-S-4P-S2T2-EF	4P	connector pin header
13439332	IL-S-5P-S2T2-EF	5P	connector pin header
13439296	IL-S-7P-S2T2-EF	7P	connector pin header
13439297	IL-S-8P-S2T2-EF	8P	connector pin header
13439345	IL-S-9P-S2T2-EF	9P	connector pin header
13439337	IL-S-13P-S2T2-EF	13P	connector pin header
13439338	IL-S-14P-S2T2-EF	14P	connector pin header
13439339	IL-S-15P-S2T2-EF	15P	connector pin header
13429191		34P	memory card

MISCELLANEOUS

23455314	Grounding Leaf (to Front Holder)
22265226	Dust Cover (to Front Panel)
22245463	LCD Dust Cover
2215040100	Joint (to button)
2215040200	Joint (to switch)
2214020700	Connection Rod
22195450	LED Holder (1 set = triplet)

BATTERY

12569249	CR2032 leadless	lithium
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MEMORY CARD

12379401	PN-D50-00 ROM	accessory
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IC DATA

CPU
μPD78312

TOP VIEW

PCM ROM A/B
TC532000

TOP VIEW

EP ROM
MBM27C512

TOP VIEW

S RAM
HM6264ASP

TOP VIEW

S RAM
HM62256LP

TOP VIEW

6N137

TOP VIEW

μPC4062G
μPC4570G
M5238FP

TOP VIEW

No	NAME	I/O	No	NAME	I/O	No	NAME	I/O	No	NAME	I/O	No	NAME	I/O
1	P0.0	O	17	NMI	I	33	AN0	I	49	A14	O			
2	P0.1	O	18	INT0	I	34	AN1	I	50	A15	O			
3	P0.2	O	19	INT1	I	35	AN2	I	51	EA	I			
4	P0.3	O	20	INT2	I	36	AN3	I	52	RESET	I			
5	P0.4	O	21	TxD	O	37	AVREF	O	53	RD	O			
6	P0.5	O	22	RxD	I	38	AVss	-	54	WR	O			
7	P0.6	O	23	SCR	O(ONC)	39	P3.4	I/O(ONC)	55	ALE	O			
8	P0.7	O	24	CTS	I/O	40	P3.5	I/O(ONC)	56	AD0	I/O			
9	P1.0	I/O	25	RFSH	O(ONC)	41	P3.6	I/O	57	AD1	I/O			
10	P1.1	I/O	26	P3.0	I	42	P3.7	I/O	58	AD2	I/O			
11	P1.2	I/O	27	P3.1	I	43	A8	O	59	AD3	I/O			
12	P1.3	I/O	28	P3.2	I	44	A9	O	60	AD4	I/O			
13	P1.4	I/O	29	P3.3	I	45	A10	O	61	AD5	I/O			
14	P1.5	I/O	30	X1	I	46	A11	O	62	AD6	I/O			
15	P1.6	I/O	31	X2	I	47	A12	O	63	AD7	I/O			
16	P1.7	I/O(ONC)	32	Vss	-	48	A13	O	64	VDD	-			

D/A CONVERTER
PCM54

TOP VIEW

D RAM
MB81416

TOP VIEW

M5F78M12
(M5F79M12)

FRONT VIEW

μPC4570HA

M5216L

74HC00

TOP VIEW

74HC10

TOP VIEW

74HC139

TOP VIEW

74HC174

TOP VIEW

HD 74LS04P

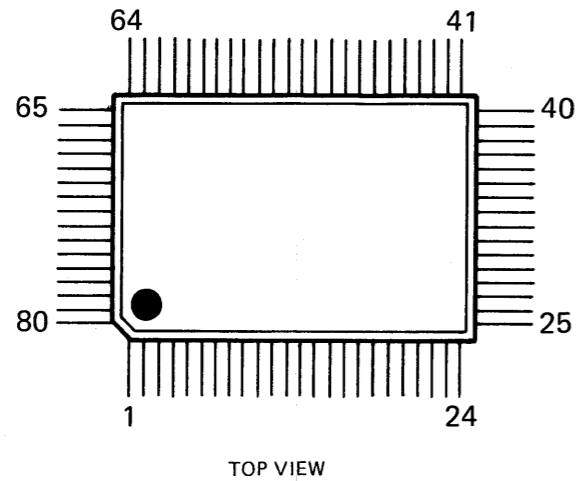
TOP VIEW

L78MR05R

FRONT VIEW

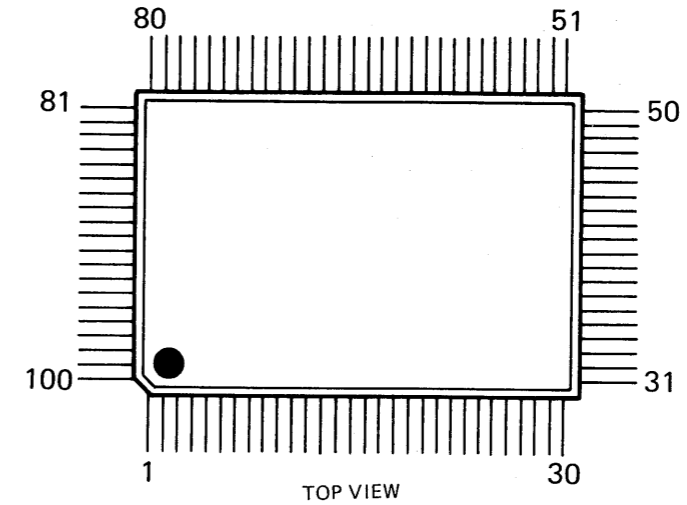
IC DATA

**REVERB CUSTOM IC
MB87126-006**



PIN.NO.	PIN NAME	I/O	DESCRIPTION	PIN.NO.	PIN NAME	I/O	DESCRIPTION
1, 2, 66~72, 74~80	DC0-1S	O	Data output for chorus chip and DAC D/A へのデータ、コーラス・データ出力端子	20	LOAD	O	Sync signal output シンク信号出力端子
3	STRT	I	Pulled low GND にプルダウン	21	SYNC	I	Sync signal input シンク信号入力端子
4	DIN	I	Pulled low GND にプルダウン	22	INCK	I	Data latch clock input for initialization イニシャライズ時のデータ・ラッチ・クロック入力端子
5	CLEA	I	Pulled low GND にプルダウン	23	ERCL	I	Busy veset output Busy 解除用端子
6~10	RDO-4	O	Control output for enable and for S/H and Lower for bit D/A Conversion コントロール出力端子 イネーブル、S/H、D/A (下4 bit)	24	BUSY	O	Serial data transfer error output (Parity check) シリアル・データ転送エラー出力 (パリティ・チェック)
11	RSET	I	Pulled low GND にプルダウン	25	SXD	I	Serial data input シリアル・データ入力端子
12, 15, 36, 52, 65	Vss	-	GND	26	SCK	I	Serial data read-in clock input シリアル・データ取込みクロック入力端子
13	SLRQ	I	Pulled low GND にプルダウン	27-32, 34, 35	DAO-7	O	Connect to RAM address bus RAM アドレス・バス
14	MSCK	I	Master clock input マスター・クロック入力端子	37	RAS	O	Row address strobe output ロー・アドレス・ストロブ
16	SLCK	O	Not used 未使用	38	WE	O	DRAM write pulse output DRAM ライト・パルス出力端子
17	TEST	I	Pulled low GND にプルダウン	39	CAS	O	Column address strobe output カラム・アドレス・ストロブ
18	TMB	O	Time base signal output タイム・ベース信号出力端子	40-51, 53-64	DRO-23	I/O	Connect to RAM data bus, Synth and Chorus data input/output RAMデータ・バス、シンセ、コーラスデータ入出力端子
19, 33, 73	VDD	-	+5V				

**CHORUS CUSTOMIC
MB87137**



PIN.NO.	PIN NAME	I/O	DESCRIPTION	PIN.NO.	PIN NAME	I/O	DESCRIPTION
1	RES	I	Reset input : pulled up to VDD リセット入力端子 VDDにプルアップ	61	WE	O	SRAM write pulse output SRAM 用 ライト・パルス出力端子
2	E	I	Chip enable input : pulled up to VDD チップ・イネーブル入力端子 VDDにプルアップ	71	OE	O	SRAM out enable output SRAM 用 アウトプット・イネーブル出力端子
3, 28, 53, 78	VDD	-	+5V	75	CE	O	SRAM chip enable output SRAM 用 チップ・イネーブル出力端子
4	CS	I	Chip select input : pulled up to VDD チップ・セレクト入力端子 VDDにプルアップ	77	PD7-O	I/O	Connect to SRAM data bus SRAM データ・バス
5	RW	I	Write pulse input ライト・パルス入力端子	88	X1	I	Master clock input マスター・クロック入力端子
6	RD	I	Read pulse input リード・パルス入力端子	89	X2	O	Not used 未使用
7	CS	I	Chip select input チップ・セレクト (LOW) 入力端子	91	ROMT	I	Pulled low テスト端子 GND にプルダウン
8-10	A0-2	I	Connect to CPU address bus CPU とのアドレス・バス	92	RAMT	I	
11-14, 16-19, 15, 40, 65, 87, 90	D0-7 Vss	I/O -	Connect to CPU data bus CPU とのデータ・バス GND	93	CTR1	I	
20	DOE	I	Data out enable input データ・アウトプット・イネーブル入力端子	94	THRU	I	
21	INCK	I	Input data latch clock input データ入力用ラッチクロック入力端子	95	ECTL	I	External control select input : pulled up to VDD エクスターナル・コントロール・セレクト入力端子 VDDにプルアップ
22	SIN	I	Sync input : pulled up to VDD シンク信号入力端子 VDDにプルアップ	96	ADDA	I	Pulled low テスト端子 GND にプルダウン
23	SOUT	O	Sync output シンク信号出力端子	97	OFST	I	OFFset binary select input : pulled up to VDD オフセット・バイナリー・セレクト VDDにプルアップ
24	LRS	I	L/R select input L/R セレクト	98	PSFT	I	Pulled low テスト端子 GND にプルダウン
25-27, 29-39, 41-42, 43-52, 54-59	IO-15 O0-15	I O	Data input データ入力端子 データ出力端子	99	LHLD	O	Signal output for S/H : not used S/H 用信号出力端子 未使用
60, 62-64, 66-70, 72-74, 76-79	RAO-13	O	Connect to SRAM address bus RA13 not used SRAM アドレス・バス RA13 未使用	100	RHLD	O	Signal output for S/H : not used S/H 用信号出力端子 未使用

IC DATA

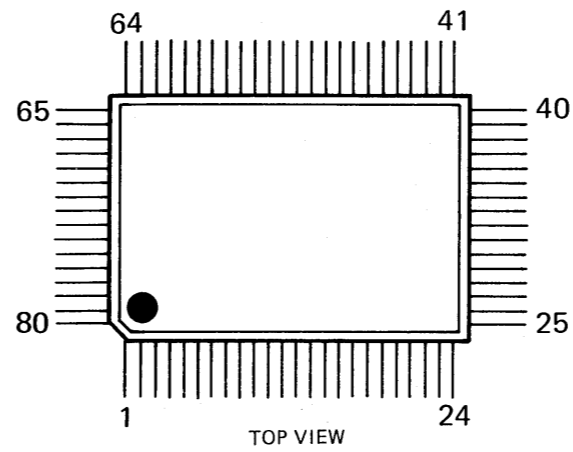
**SYNTH CUSTOMIC
MB87136**

34	33	32	31	30	29	28	27	26	25	24	23
35	72	71	70	69	68	67	66	65	64	63	22
36	73				86	85				62	21
37	74									61	20
38	75									60	19
39	76	87							84	59	18
40	77	88							83	58	17
41	78									57	16
42	79									56	15
43	80				81	82				55	14
44	45	46	47	48	49	50	51	52	53	54	13
1	2	3	4	5	6	7	8	9	10	11	12

INDEX PIN TOP VIEW

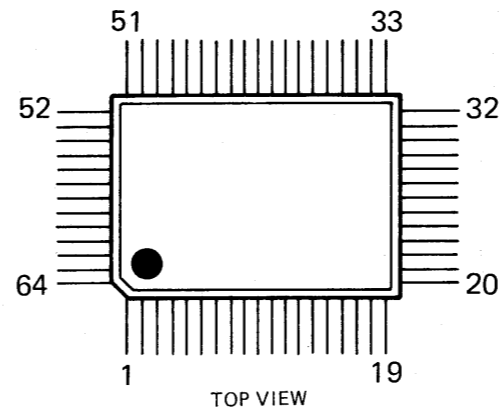
PIN NO.	PIN NAME	I/O	DESCRIPTION	PIN NO.	PIN NAME	I/O	DESCRIPTION
1	CS	I	Chip select チップ・セレクト入力端子	44	INT	O	Interrupt output インタラプト 出力端子
2 - 6, 46 - 49	A0-8	I	Connect to CPU address bus CPU とのアドレス・バス	45	OE	I	Output enable input アウトプット・イネーブル入力端子
7 - 10, 50 - 53	D0-7	I/O	Connect to CPU data bus CPU とのデータ・バス	75		-	Not used 未使用
11 - 14, 54 - 57	PD0-7	I	Connect to ROM data bus ROM とのデータ・バス	76	X2	I/O	Xtal input 水晶振動子 (32.768 MHz) 接続端子
15 - 26, 58 - 65	RA0-19	O	Connect to ROM address bus ROM とのアドレス・バス	77	16M	O	Output frequency is one half of master clock マスター・クロックを1回分周した周波数を出力
27 - 35, 66 - 72	Q0-15	O	Data output データ・アウトプット・バス	78	CKIN	I	Output frequency is a combination of the master clock and one half of master clock マスター・クロックと1回分周した周波数を入力
36 - 37, 73 - 74	SH0-3	O	Not used 未使用	79		-	Not used 未使用
38		-	Not used 未使用	80	RD	I	Read pulse input リード・パルス入力端子
39	X1	I/O	Xtal input (32.768 MHz) 水晶振動子 (32.768 MHz) 接続端子	81, 84, 85, 88,	Vss	-	GND
40	32M	O	The same frequency as that of master clock マスター・クロックと同じ周波数を出力	82, 83, 86, 87,	VDD	-	+5 V
41		-	Not used 未使用				
42	SYI	I	Sync signal input シンク信号入力端子				
43	WR	I	Write pulse input ライト・パルス入力端子				

**GATE ARRAY
HG61H25B18F**



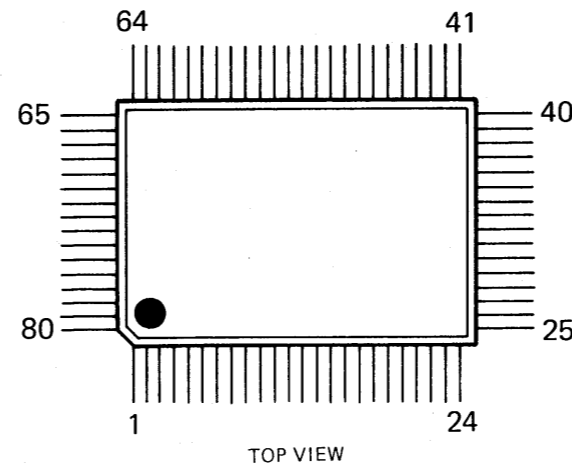
PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	SYNT2	O (NC)	21	ALE	I	41	EC	O	61	R2	I
2	IRAM	O (NC)	22	WR	I	42	O0	O	62	R3	I
3	RAM	O	23	RD	I	43	O1	O	63	R4	I
4	A7	O	24	RESET	I	44	O2	O	64	R5	I
5	A6	O	25	A15	I	45	O3	O	65	R6	I
6	A5	O	26	A14	I	46	O4	O	66	R7	I
7	A4	O	27	A13	I	47	O5	O	67	CORUS	O
8	A3	O	28	A12	I	48	O6	O	68	SCK	O
9	A2	O	29	A11	I	49	O7	O	69	SXD	O
10	A1	O	30	A10	I	50	S0	O	70	BUSY	I
11	A0	O	31	A9	I	51	S1	O	71	ERCL	O
12	Vss	-	32	A8	I	52	Vss	-	72	LOAD	I
13	AD7	I/O	33	Vdd	-	53	S2	O	73	Vdd	-
14	AD6	I/O	34	ARS	I (HIGH)	54	S3	O	74	TMB	I
15	AD5	I/O	35	INT1	O (NC)	55	S4	O	75	SINT1	I (LOW)
16	AD4	I/O	36	INT2	O	56	S5	O	76	SINT2	I (LOW)
17	AD3	I/O	37	DSCAN	O	57	S6	O	77	TEST1	I (LOW)
18	AD2	I/O	38	ERAM	O	58	S7	O	78	CLK	I
19	AD1	I/O	39	ERAM	O (NC)	59	R0	I	79	TEST2	I (LOW)
20	AD0	I/O	40	RS	O	60	R1	I	80	SYNT1	O

**GATE ARRAY
μPD65005G-062**



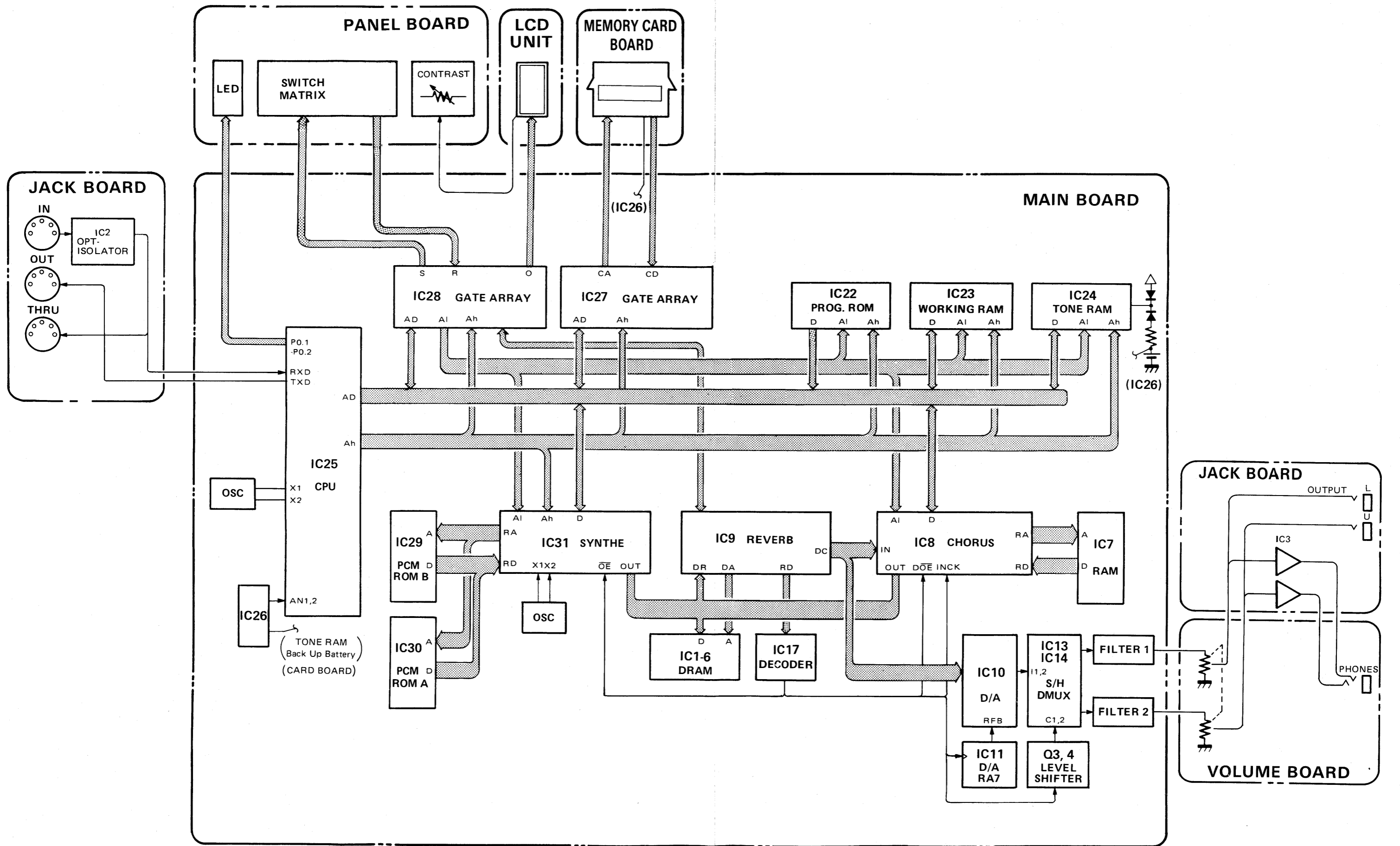
PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	NC	-	17	NC	-	33	NC	-	49	NC	-
2	NC	-	18	NC	-	34	NC	-	50	CD0	I/O
3	AD7	I/O	19	A13	I	35	CA5	O	51	CD1	I/O
4	AD6	I/O	20	A12	I	36	CA6	O	52	CD2	I/O
5	AD5	I/O	21	A11	I	37	CA7	O	53	CD3	I/O
6	AD4	I/O	22	A10	I	38	CA8	O	54	CD4	I/O
7	AD3	I/O	23	A9	I	39	CA9	O	55	CD5	I/O
8	AD2	I/O	24	A8	I	40	CA10	O	56	CD6	I/O
9	AD1	I/O	25	SEL	I (LOW)	41	CA11	O	57	CD7	I/O
10	AD0	I/O	26	Vss	-	42	CA12	O	58	Vss	-
11	Vss	-	27	Vdd	-	43	CA13	O	59	Vdd	-
12	Vdd	-	28	CA0	O	44	CA14	O	60	BATT	I (LOW)
13	ALE	I	29	CA1	O	45	MR	O	61	SENS	I (NC)
14	WR	I	30	CA2	O	46	CWR	O	62	RCS	I
15	RD	I	31	CA3	O	47	CCS	O	63	CS	I
16	A14	I	32	CA4	O	48	CRD	O	64	NC	-

**GATE ARRAY
MB63H149**

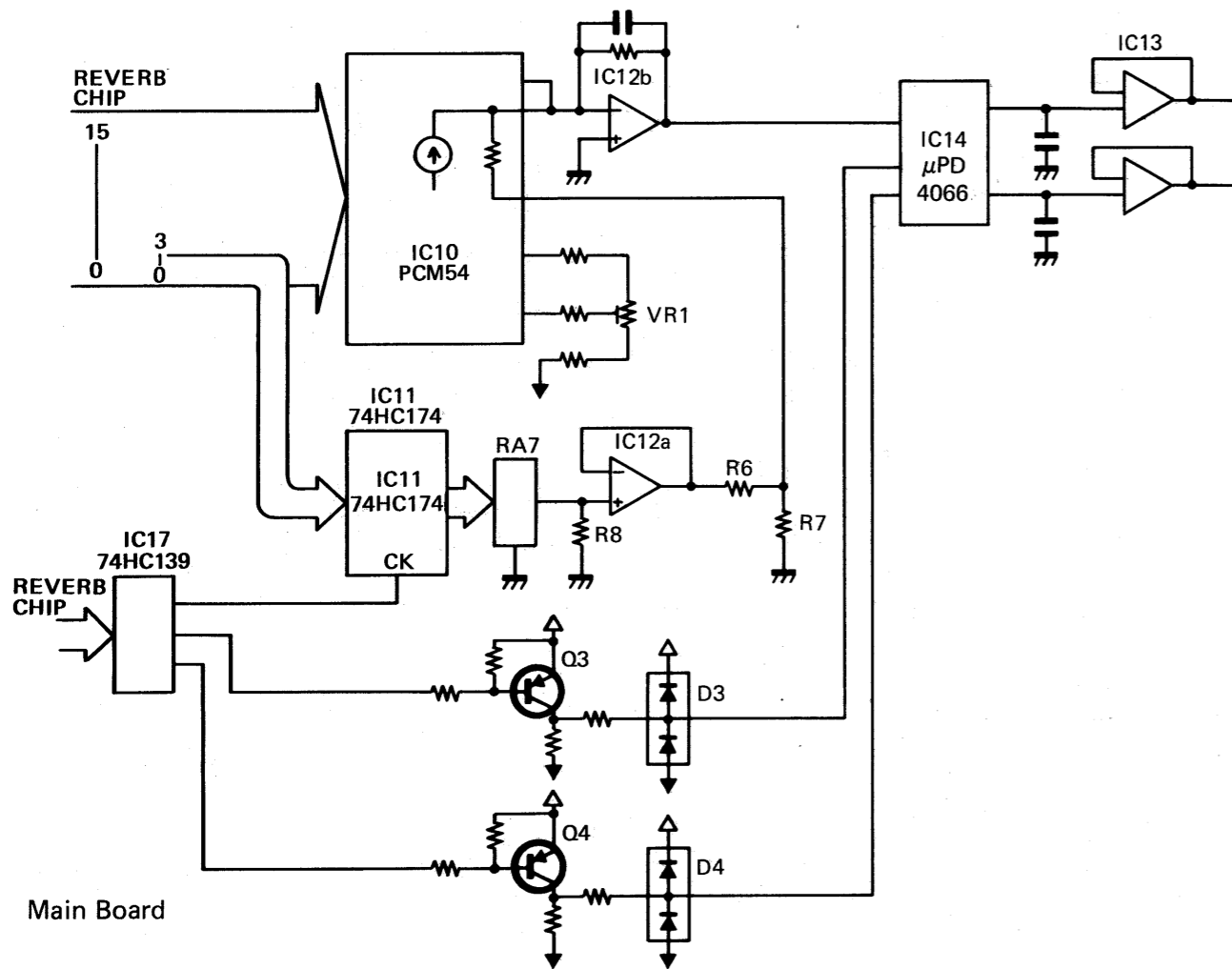


PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O	PIN NO.	NAME	I/O
1	T7	O	21	BR9	I	41	AD7	I/O	61	RA1	O
2	BR0	I	22	MK9	I	42	CA8	I	62	RA10	O
3	MK0	I	23	BR10	I	43	CA9	I	63	RA2	O
4	BR1	I	24	MK10	I	44	CA10	I (LOW)	64	ROE	I/O
5	MK1	I	25	RES	I	45	CS	I	65	RA3	O
6	BR2	I	26	EXCK	I/O	46	XT1	I	66	RWE	O
7	MK2	I	27	E	I (HIGH)	47	XT2	O (NC)	67	RA4	O
8	BR3	I	28	INT	O	48	ASEL	O (NC)	68	RA9	O
9	MK3	I	29	AS	I	49	MOD1	I (HIGH)	69	RA5	O
10	BR4	I	30	CRES	O (NC)	50	MOD2	I (LOW)	70	RA8	O
11	MK4	I	31	CRNW	I	51	RD3	I/O	71	RA6	O
12	Vss	-	32	SRCK	O (NC)	52	Vss	-	72	RA7	O
13	BR5	I	33	Vdd	-	53	RD4	I/O	73	Vdd	-
14	MK5	I	34	AD0	I/O	54	RD2	I/O	74	T0	O
15	BR6	I	35	AD1	I/O	55	RD5	I/O	75	T1	O
16	MK6	I	36	AD2	I/O	56	RD1	I/O	76	T2	O
17	BR7	I	37	AD3	I/O	57	RD6	I/O	77	T3	O
18	MK7	I	38	AD4	I/O	58	RD0	I/O	78	T4	O
19	BR8	I	39	AD5	I/O	59	RD7	I/O	79	T5	O
20	MK8	I	40	AD6	I/O	60	RA0	O	80	T6	O

D-550 BLOCK DIAGRAM



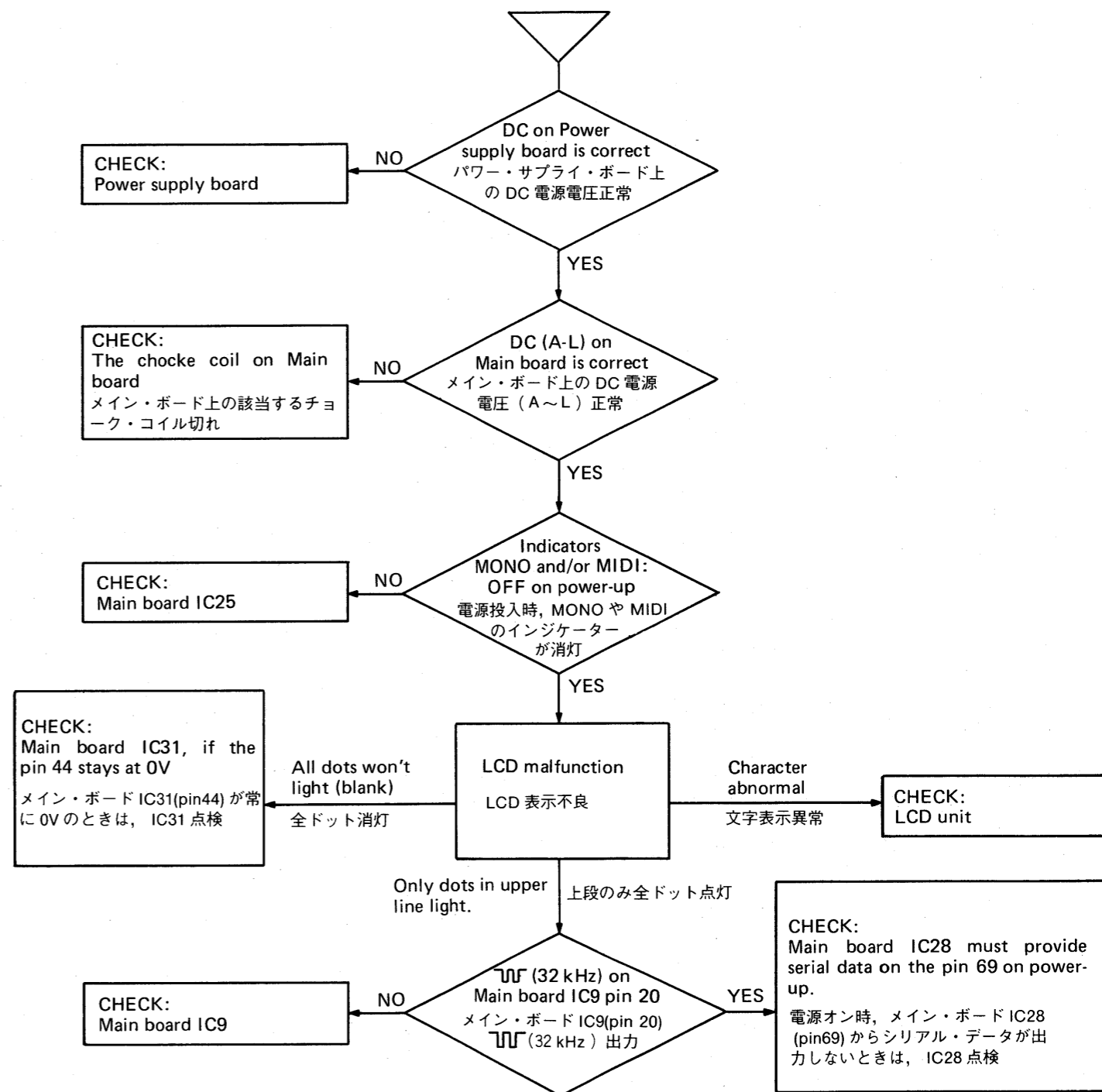
Digital to Analog Conversion (20bits)



IC10	Upper 16 bits D/A Conversion 上位16 bit D/A 変換
IC11	Lower 4 bits data latch 下位 4 bit データ・ラッチ
RA7	Lower 4 bits D/A Conversion 下位 4 bit D/A 変換
IC12a R6 R7 R8	Lower 4 bits Weighing 下位 4 bit の重み付け
VR1	MSB Weight adjuster MSB 重み調整
IC12b	I/V Conversion I/V 変換
IC14	Analog switch ; separates UPPER and LOWER UPPER と LOWER の信号に分ける アナログ・スイッチ
Q3, D3 Q4, D4	LEVEL SHIFTER
IC17	DECODER
IC13	S/H

TROUBLESHOOTING LOGIC TREE / 暴走時のトラブル・ガイド

The below will help in some failure conditions.
暴走時、下記のチェックである程度の不良箇所を推測することができる。



IDENTIFYING ROM (IC22) VERSION NUMBER

Hold PATCH BANK 6, PATCH NUMBER 6 and EXIT then switch the power on. The first line of the display should show the current ROM version number, then the instrument will enter into normal play mode.

DAC ADJUSTMENT

With monitor system connected to OUTPUT jack (U or L). Start with the unit turned off.

1. Hold PATCH BANK 2, PATCH NUMBER 6 and WRITE then switch the power on. The LCD should read:

*with ROM Ver. 1.00 the display automatically shows a test title.

```
***** L.A. Chip Test Mode V70000*****
Press [COMPARE] for D/A Adjustment mode.
```

2. Press COMPARE and the instrument will enter into adjustment mode. The unit will show a test title while generating a low level test sound.

```
***** L.A. Chip Test Mode V70000*****
/*D/A Adjustment */
```

3. Raise VOLUME to top.
4. Adjust VR1 (Main board) for the minimum distortion.
5. Turn the power off.

RECOVERING TONE RAM DATA

When the backup battery or RAM (IC24) has been replaced, take the following steps. Start with unit turned off.

1. (Refer to D-550 Owner's Manual, Page 105) Transfer PATCH and REVERB TYPE (17-32) data from the Memory Card (PN-D-50-00).
2. Hold PATCH BANK 2, PATCH NUMBER 6 and ENTER, then turn the power on. TUNE/FUNCTION and MIDI function data will be stored into the RAM. The LCD will read "Complete" and then normal play mode message.

バージョン・ナンバーの確認

PATCH BANK 6 と PATCH NUMBER 6 と EXIT を押しながら、電源オン。しばらくバージョン・ナンバーが表示（ディスプレイ上段）された後、プレイ・モードの表示になる。

D/A調整

アウトプット・ジャックにアンプを接続。

- ① PATCH BANK 2 と PATCH NUMBER 6 と WRITE を押しながら電源オン。

* ROM の Ver. 1.00 のときは、直接②の画面になる。

```
***** L.A. Chip Test Mode V70000*****
Press [COMPARE] for D/A Adjustment mode.
```

- ② COMPARE を押すと、調整モードになる。（下表の表示になるとともに、微小レベルの調整音が発音される。）

```
***** L.A. Chip Test Mode V70000*****
/*D/A Adjustment */
```

- ③ VOLUME ツマミを最大にする。
- ④ VR1 で、歪が最小になるように調整。
- ⑤ 調整終了後は、電源をオフにする。

データの設定

バッテリーや TONE RAM (IC24) の交換などで、TONE RAM のデータが失われた場合に次の操作を行なう。

1. パッチやリバーブ・タイプ (17-32) のデータは、D-550 のオーナーズ・マニュアル (P 105) を参照の上、メモリー・カード (PN-D50-00) からデータの転送を行なう。
2. チューン/ファンクションや MIDI ファンクションのデータは、PATCH BANK 2 と PATCH NUMBER 6 と ENTER を押しながら、電源オンにしてイニシャライズする。Complete としばらく表示された後、プレイ・モードの表示になる。

TEST MODE

CAUTION

Leave card slot disengaged.

Hold PATCH BANK 2, PATCH NUMBER 6 and EDIT then turn the power on. The display will show Test Mode menu.

```
D-550 Test Mode.  Select Type ...
▶ Memory Panel Card
```

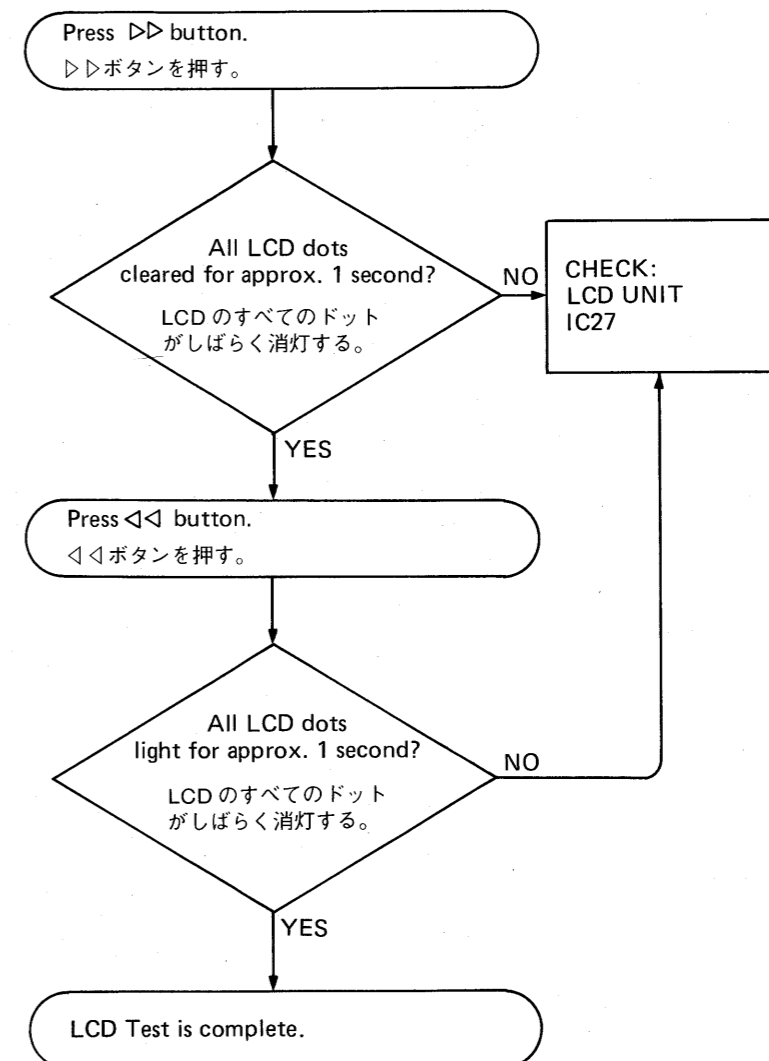
Flashing

If an error message, as shown below is displayed instead of the test mode menu, check the IC and related circuits.

"Reverb Error" → IC9 "Chorus Error" → IC8

To ignore the error, press EXIT to display the menu.

[LCD TEST]



テスト・モード

テストを行なう前は、メモリー・カードを挿入しない。

PATCH BANK 2, PATCH NUMBER 6 と EXIT を押しながら、電源を入れると、テスト・モードのメニュー画面が表示される。

```
D-550 Test Mode.  Select Type ...
▶ Memory Panel Card
```

点滅

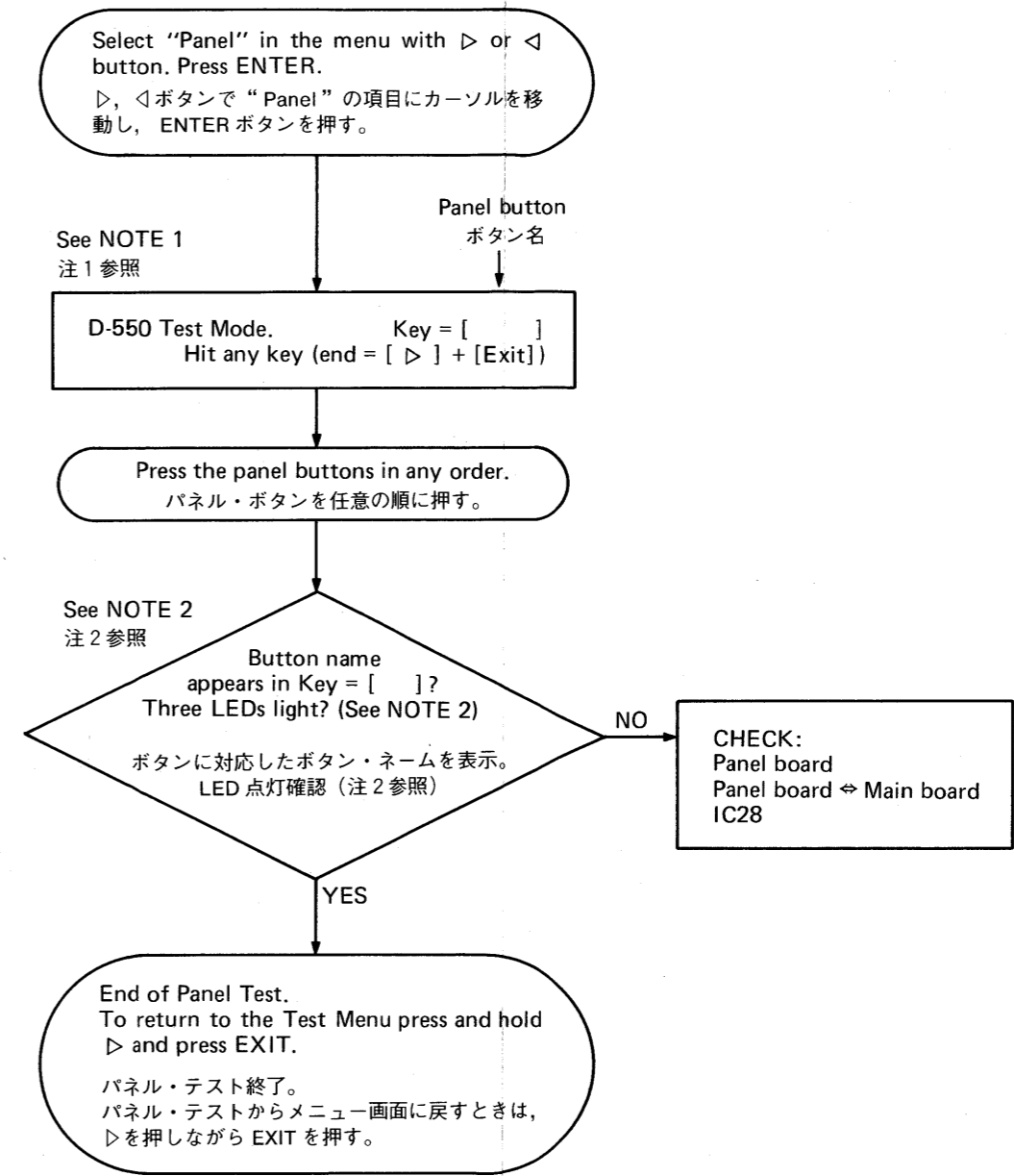
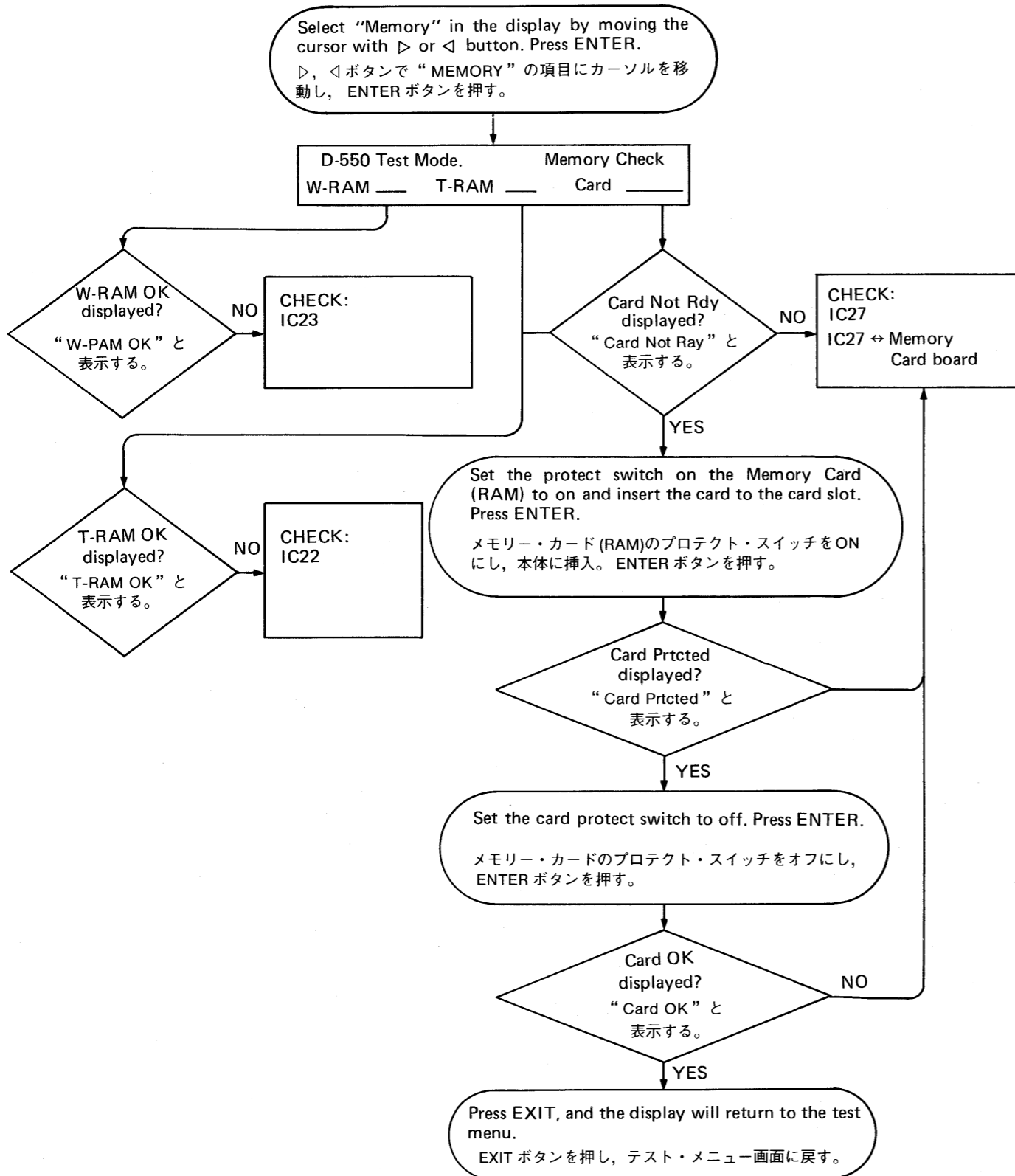
"Reverb Error!!" "Chorus Error!!" のエラー・メッセージが表示された時は、該当する IC 周辺の不良。

"Reverb Error" → IC9 "Chorus Error" → IC8

そのまま次のステップへ進む時は EXIT を押し、テスト・メニュー画面にする。

(MEMORY TEST)

(PANEL TEST)



NOTE 1:
Default values should be empty. Any figure indicates defective in corresponding circuit.

NOTE 2:
LED lights corresponding to the following button.

Button	Indicator
CHASE	CHASE
ENTER	MIDI
SHIFT	MONO

注1:
画面を呼び出した時は、ボタン名は表示されない。何らかのボタン名が表示された時は、該当する箇所をチェック。

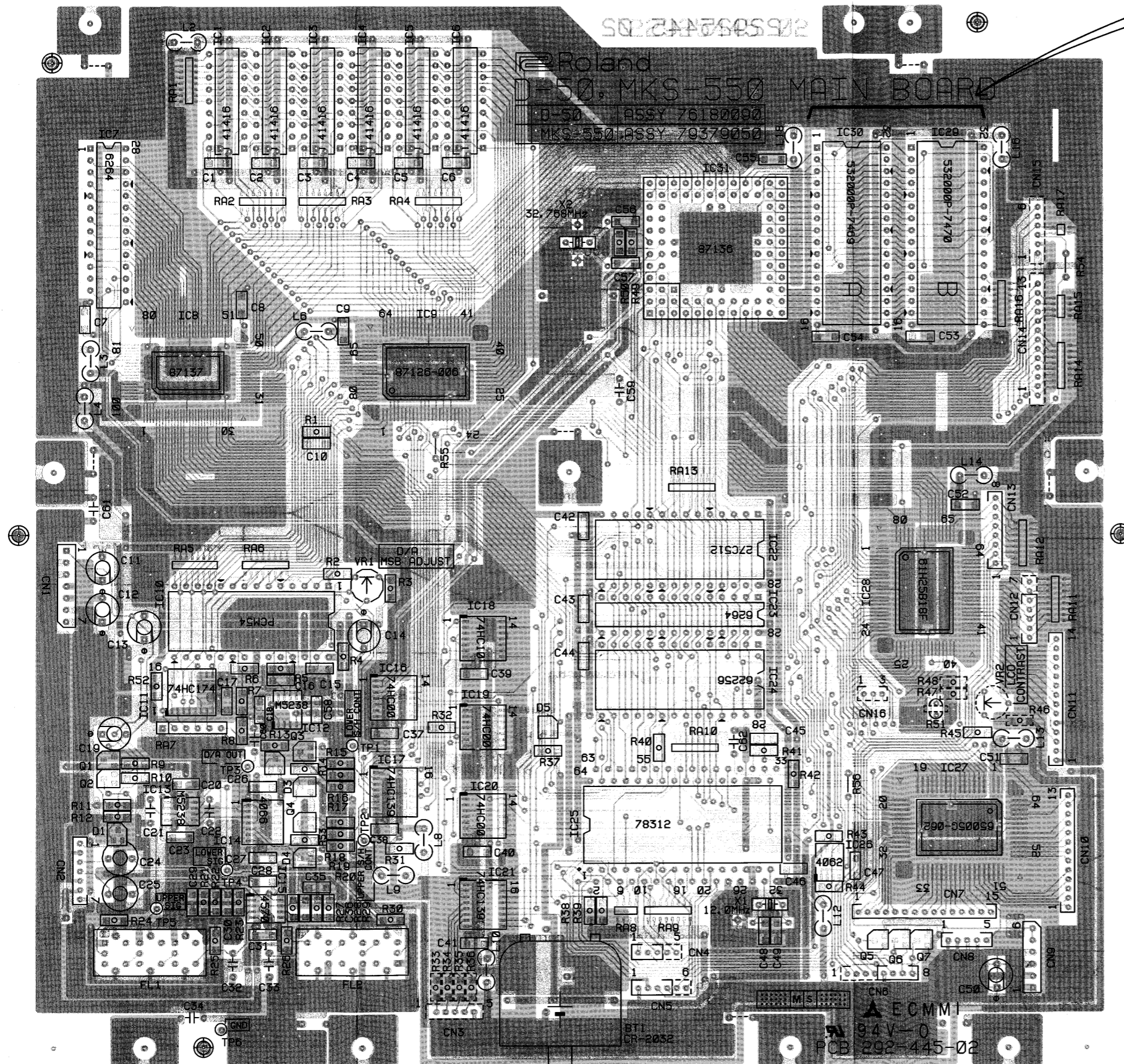
注2:
LEDは次のボタンに対応して点灯。

ボタン インジケータ	
CHASE	CHASE
ENTER	MIDI
SHIFT	MONO

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T

MAIN BOARD 76180090 (pcb 22925445)



PIGGYBACKED ROM PCB

Some PCM ROMs A (IC30) and B (IC29) are mounted on a piggybacked pcb (call this PCM ROM PCB ASSY):

They are level-for-level incompatible with regular PCM ROMs and will not work if directly installed on the main board.

When replacing, use one listed on the parts list and discard of the PCM ROM PCB ASSY.

PCM ROM A (IC30)/B (IC29)

一部のロットでは代用に、PCM ROM PCB ASSY が実装されているものがあります。

その際、PCM ROM を交換される場合は、PCM ROM PCB ASSY を取り外し、パーツ・リストに記載されている PCM ROM に交換してください。

なお、PCM ROM PCB ASSY の PCM ROM は、メイン・ボードに直接実装しても働きません。

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.
Udskiftning må kun foretages af en sagkyndig,
og som beskrevet i servicemanual.

Lithium batteri må kun udskiftes med samme type
og fabrikat.

ADVARSEL!

Lithiumbatteri. Fare for eksplotion.
Ma bare skiftes av kvalifisert tekniker som
beskrevet i servicemanualen.

Lithium batteri må kun utskiftes med samme type
og fabrikat.

VARNING!

Lithiumbatteri. Explosionsrisk.
Får endast bytas av behörig servicetekniker.
Se instruktioner i servicemanualen.

Lithium batteri för endast ersättes med samma typ
och fabrikat.

VAROITUS!

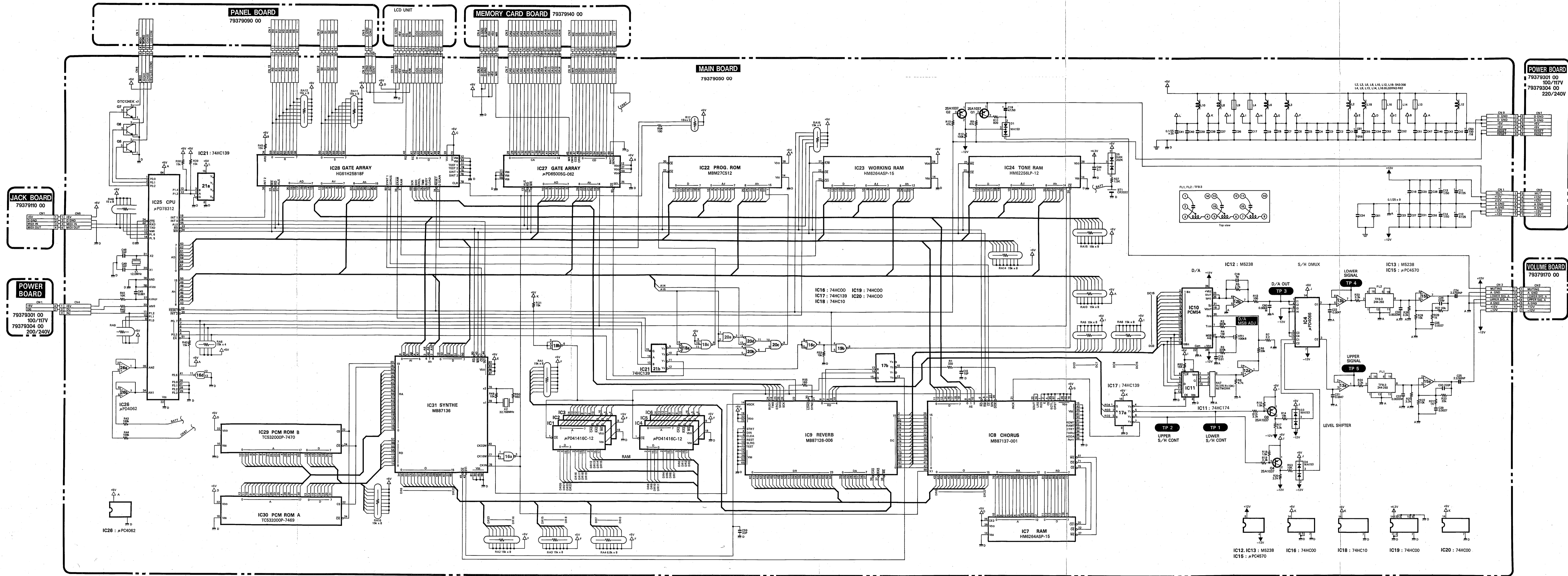
Lithiumparisto. Rajahdysvaara.
Pariston saa vaihtaa ainoastaan
alan ammottimies.

Kun vaihat lithium pariston KAYTA saman valmistajan
samaa tyyppiä.

View from component side

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70

A
B
C
D
E
F
G
H
I
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K
L
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U
V
W
X
Y
Z

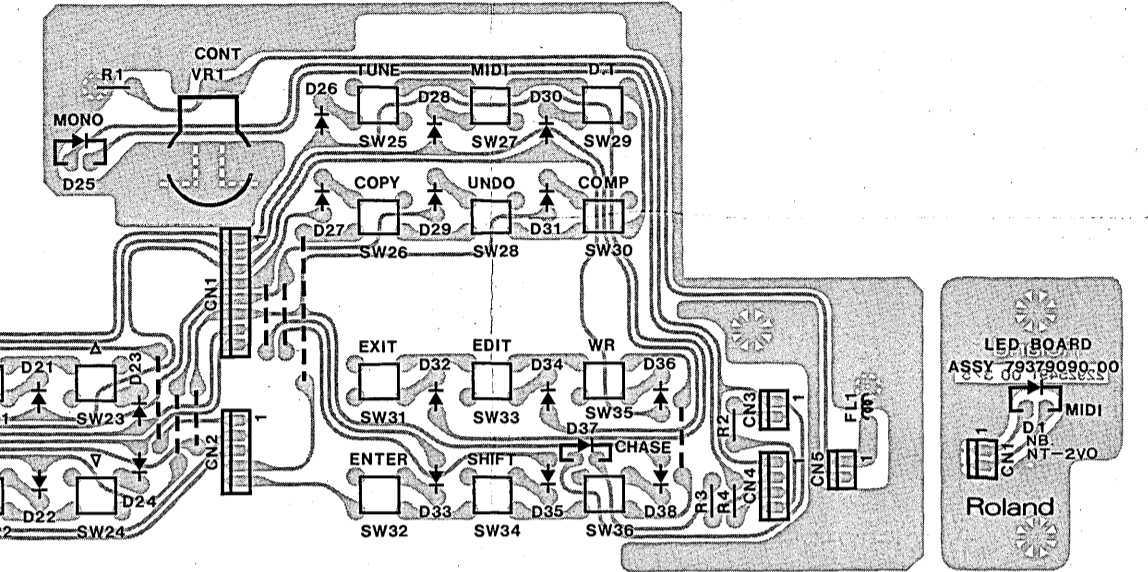
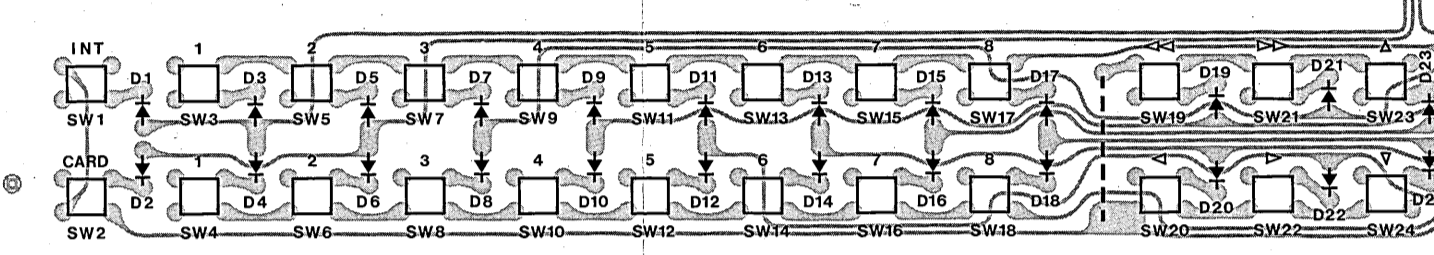


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70

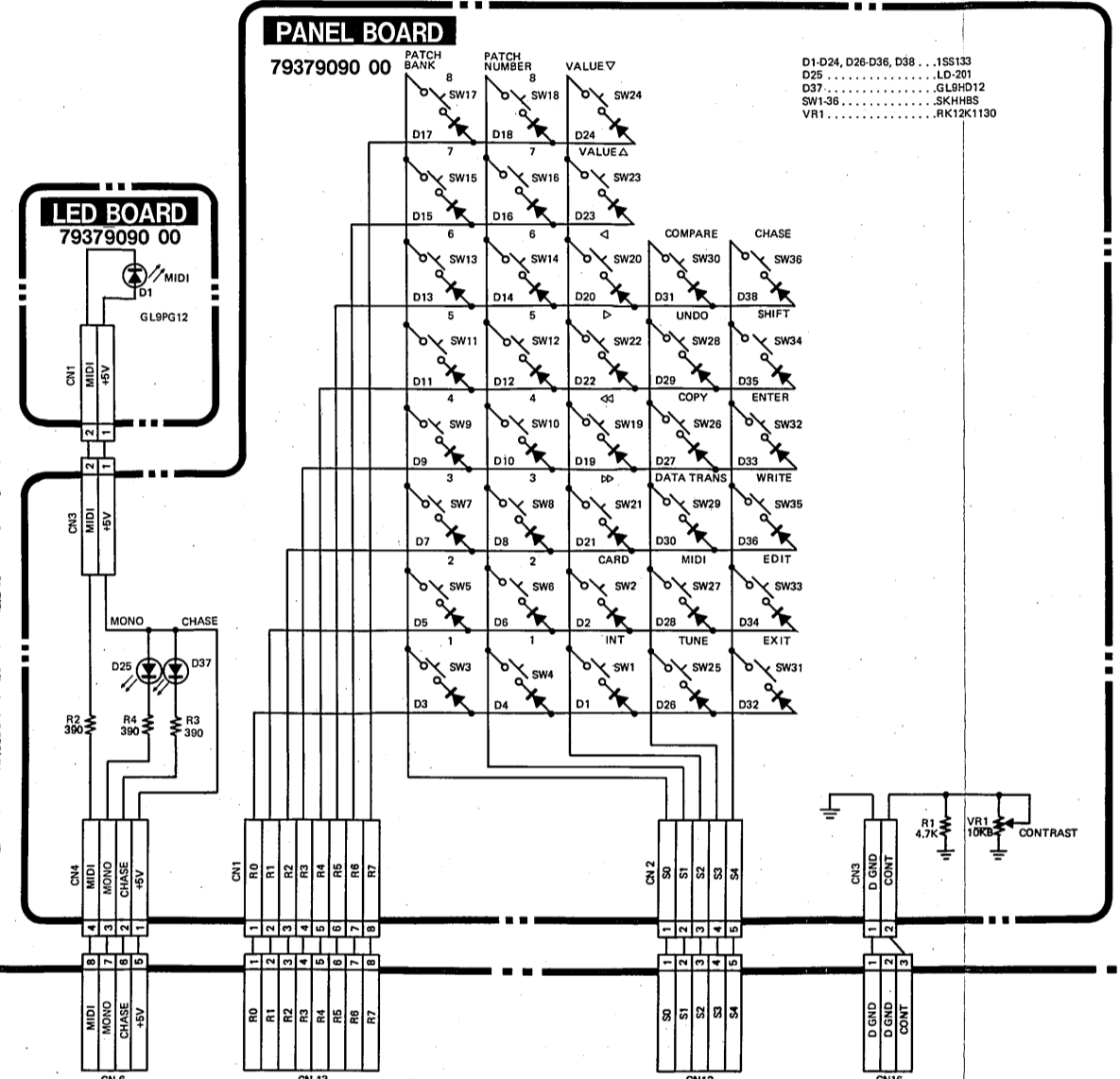
A
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L
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P
Q
R
S
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V
W
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Y
Z

PANEL/LED BOARD
79379090 00 (pcb 22925491)

Roland D-550 PANEL BOARD ASSY 79379090 00

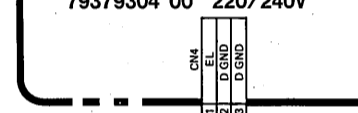


View from component side

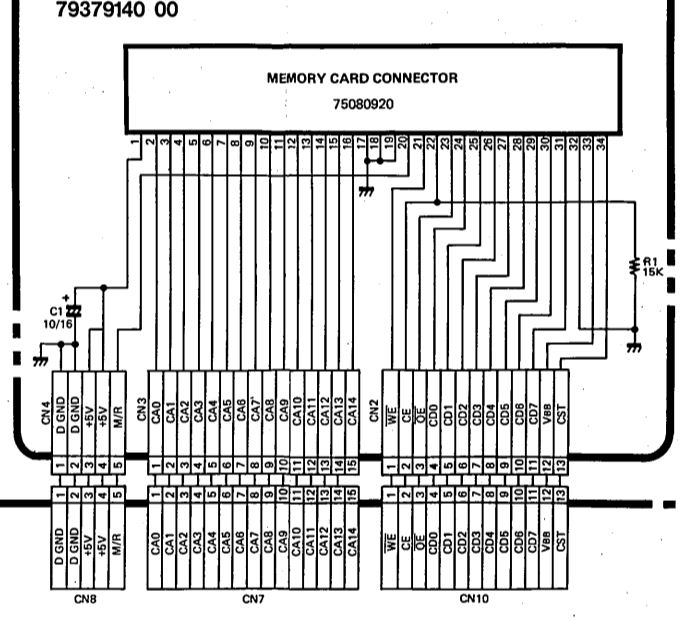


LED BOARD
79379090 00

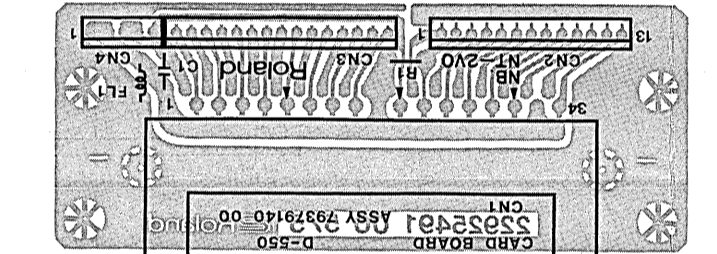
POWER SUPPLY BOARD
79379301 00 100/117V
79379304 00 220/240V



MEMORY CARD BOARD
79379140 00

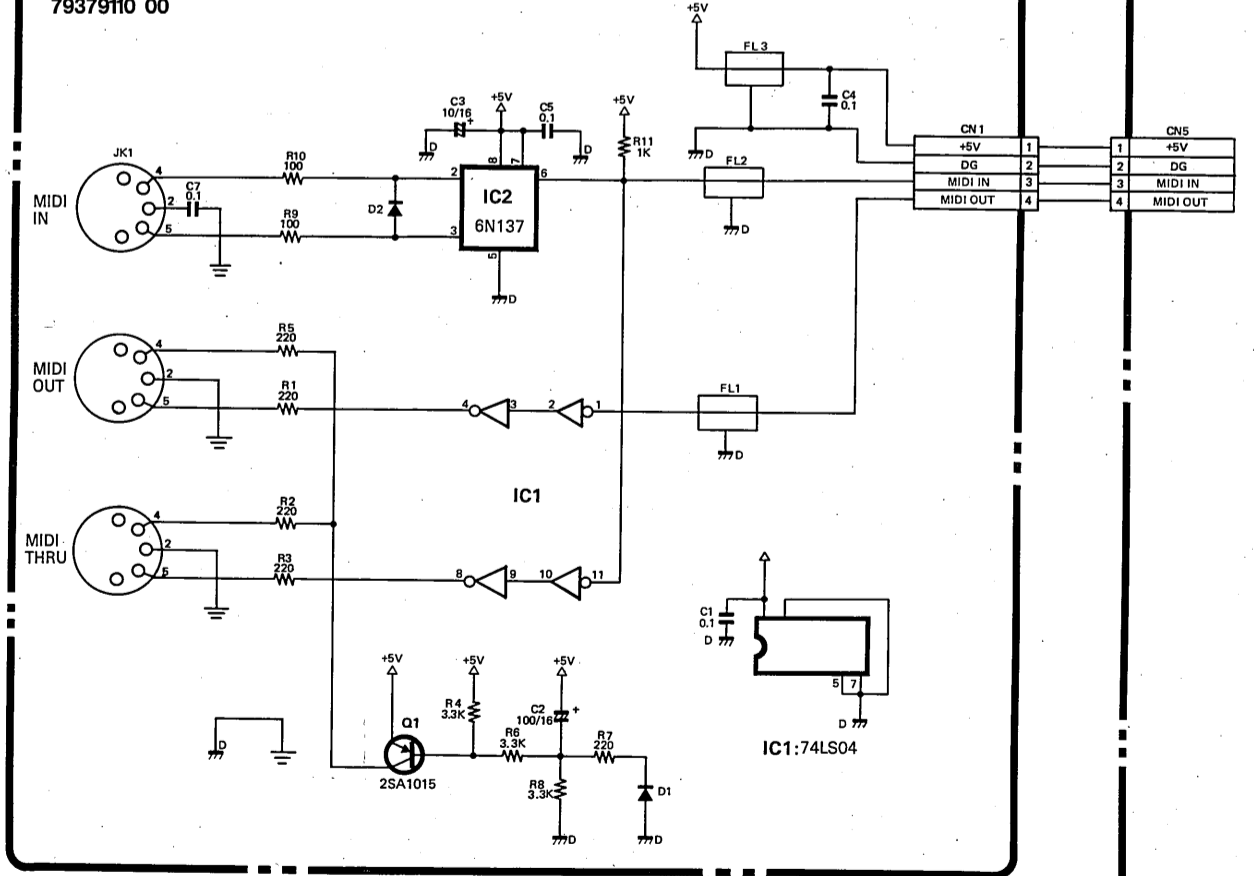


MEMORY CARD BOARD
79379140 00 (pcb 22925491)

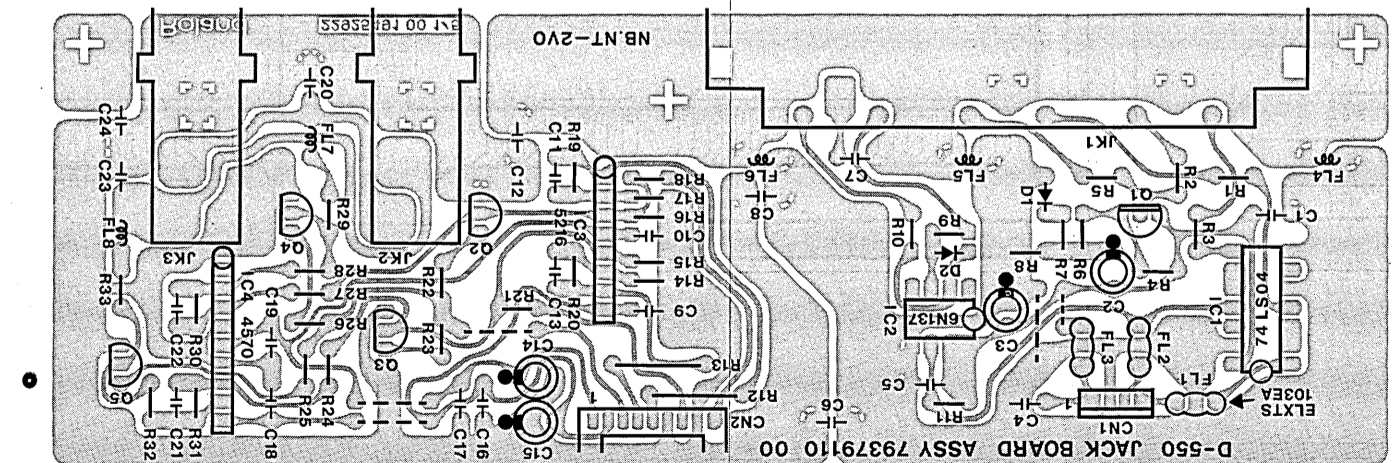


View from component side

JACK BOARD
79379110 00

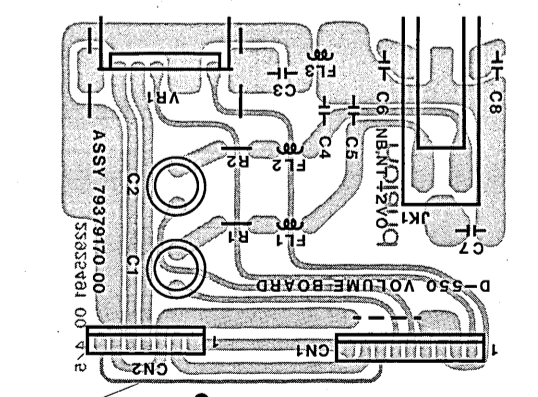


JACK BOARD
79379110 00 (pcb 22925491)



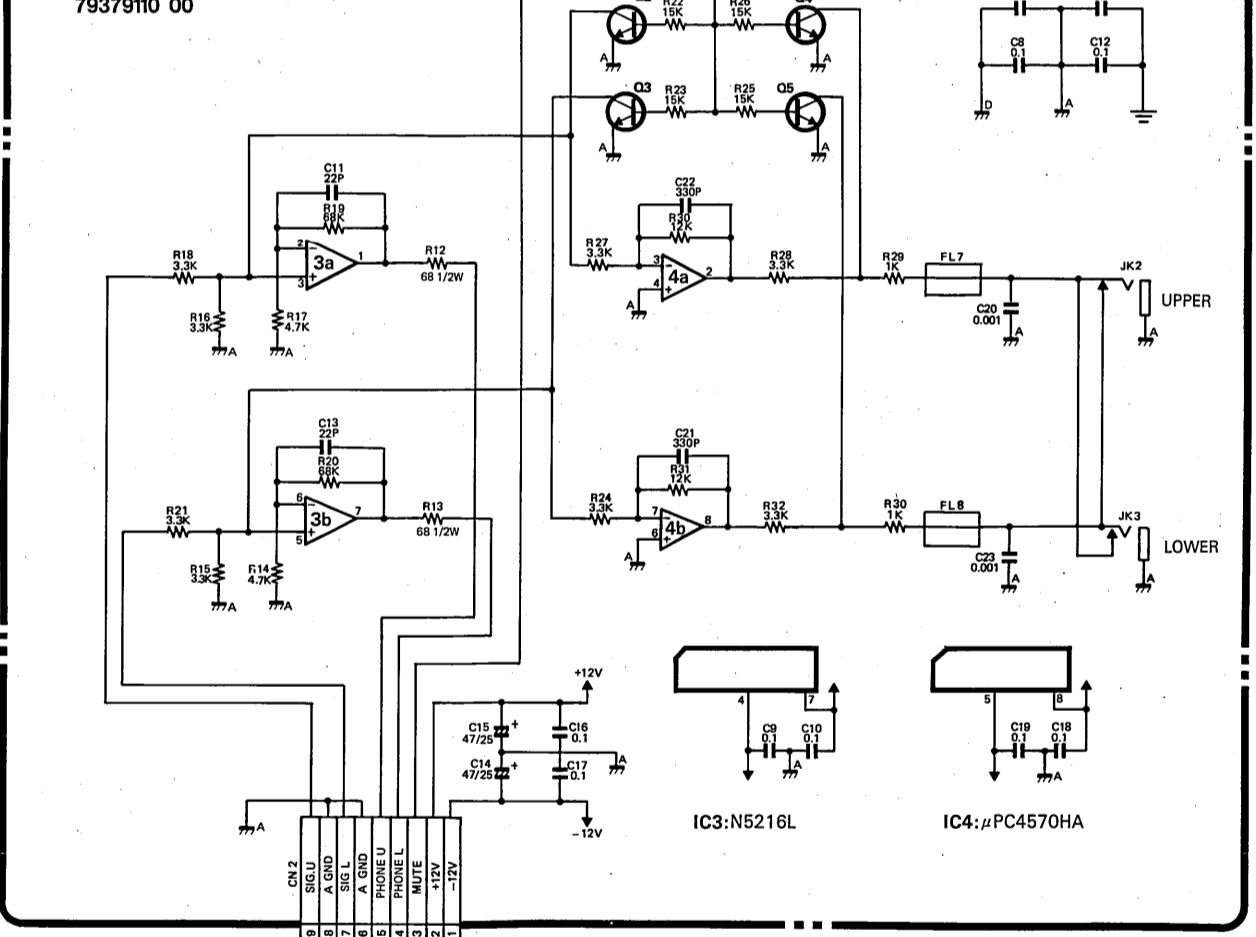
View from component side

VOLUME BOARD
79379170 00 (pcb 2295491)

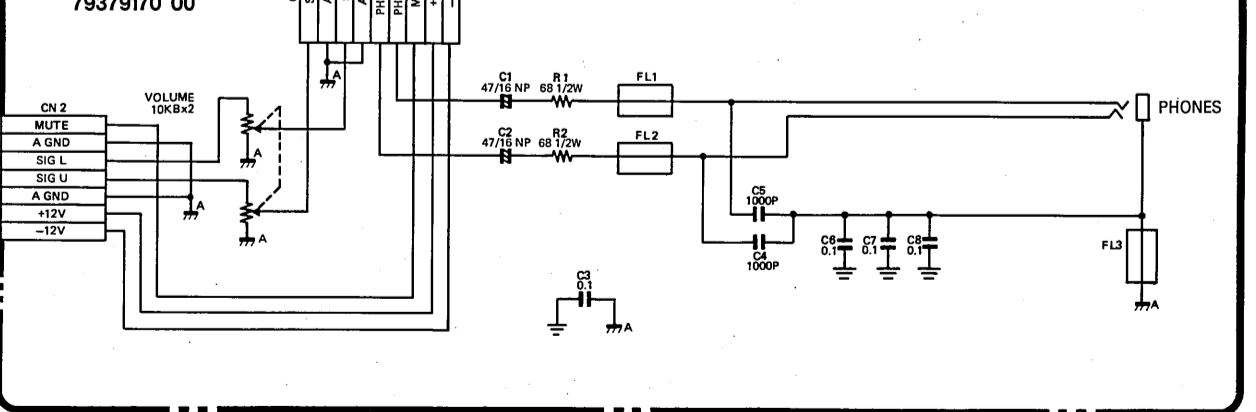


View from component side

JACK BOARD
79379110 00



VOLUME BOARD
79379170 00

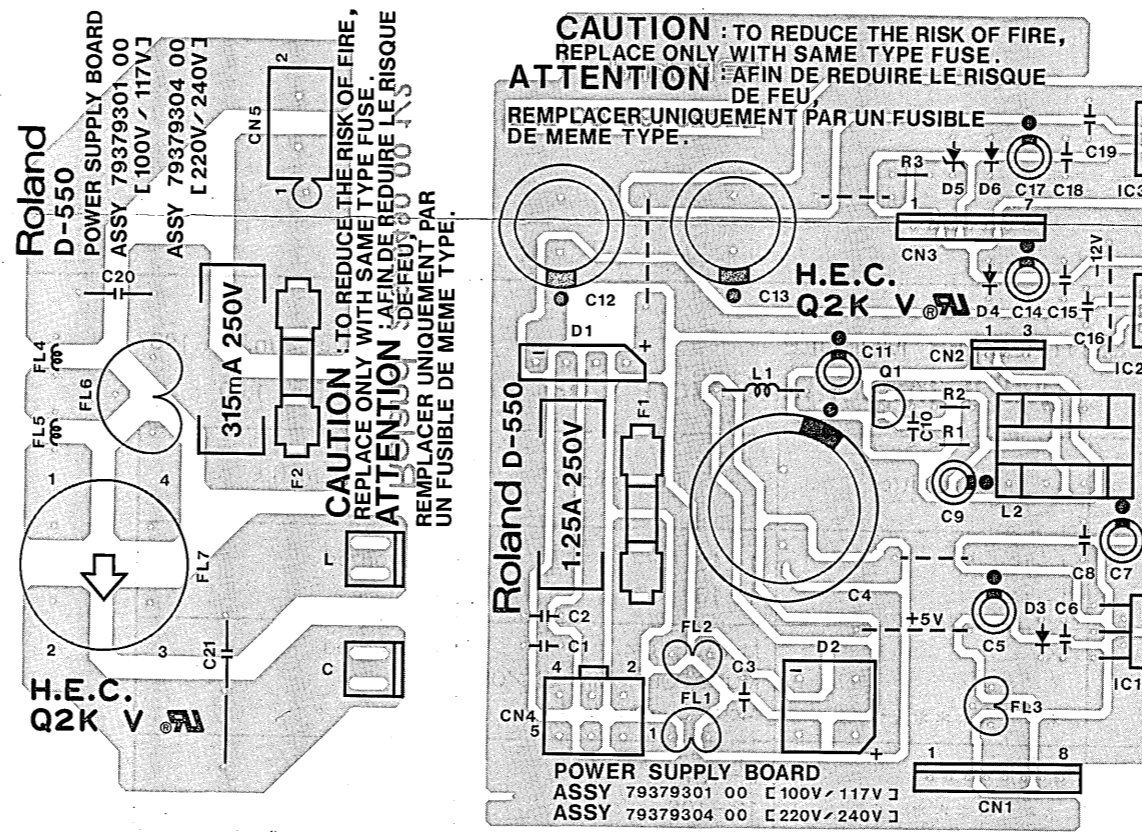


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37

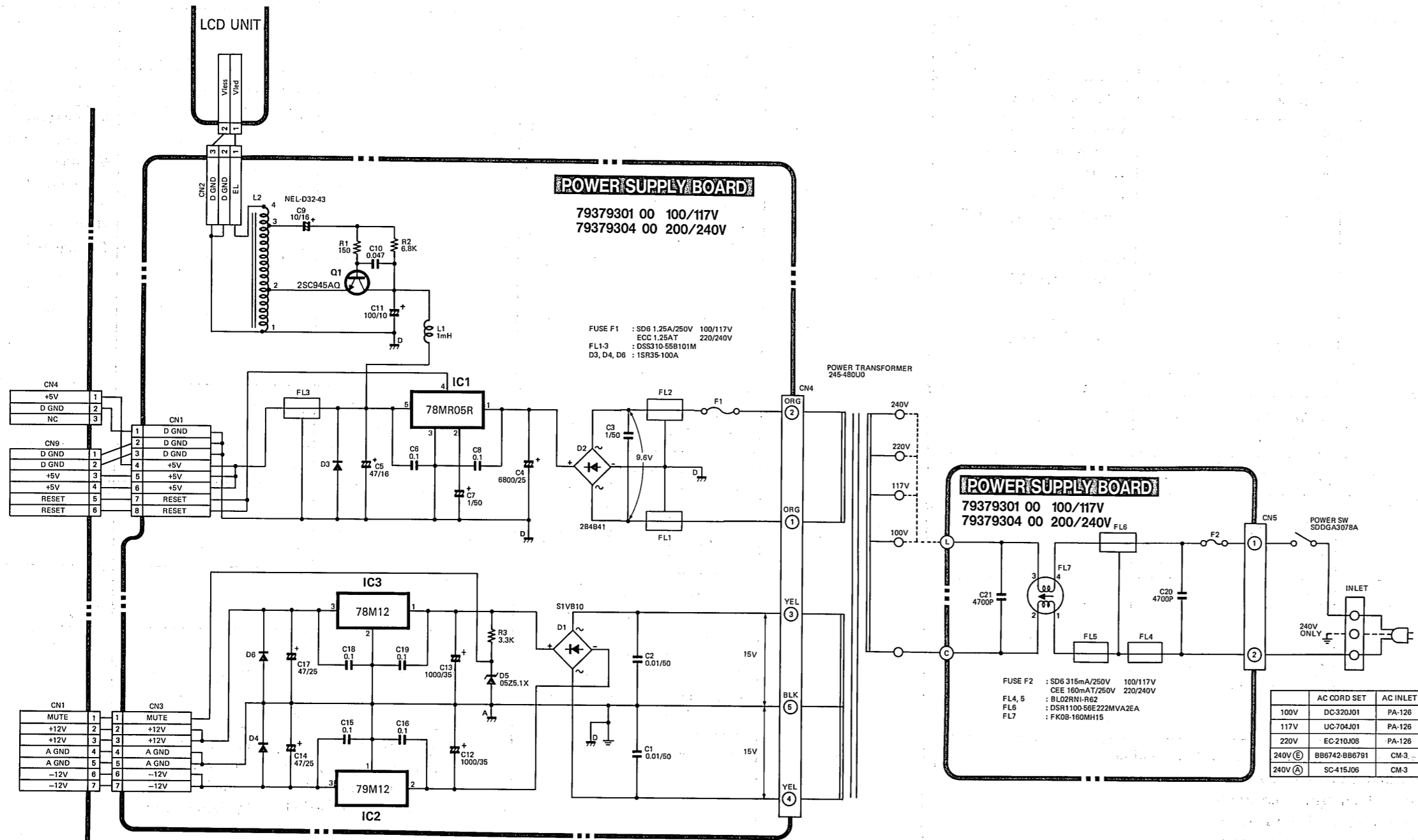
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

POWER SUPPLY BOARD

(pcb 22925490)



View from component side



8-16 VOICE LINEAR SYNTHESIZER MODULE
MODEL D-550 **MIDI Implementation Chart**

Date : Jun. 27. 1987
Version : 1.00

Function...	Transmitted	Recognized	Remarks
Basic Channel	Default Changed	1-16 1-16	Memorized
Mode	Default Messages Altered	X *****	Mode 1, 3, 4 MONO,POLY,OMNI ON/OFF Mode 2 → Mode 1 Memorized
Note Number	True Voice	X *****	0-127 12-108
Velocity	Note ON Note OFF	X X	○ v=1-127 X
After Touch	Key's Ch's	X X	X *
Pitch Bender		X	* 0-12 semi 9 bit resolution
Control Change	1	X	*
	5	X	*
	7	X	*
	0, 2-4, 8-31	X	○
	6, 38	X	**
Control Change	64	X	*
	65	X	*
	66-95	X	○
	100, 101	X	** (0, 1) RPC (LSB, MSB)
Prog Change	True #	X *****	* 0-127 0-127
System Exclusive		*	*
System Common	Song Pos	X	X
	Song sel	X	X
	Tune	X	X
System Real Time	Clock	X	X
	Commands	X	X
Aux Message	Local ON/OFF	X	X
	All Notes OFF	X	○ (123-127)
	Active Sense	X	○
	Reset	X	X
Notes			* Can be set to ○ or X manually, and memorized. ** RPC=Registered parameter control number. RPC#0 : Pitch bend sensitivity RPC#1 : Master fine tuning Parameter values are given by Data Entry.

Mode 1 : OMNI ON, POLY
Mode 3 : OMNI OFF, POLY

Mode 2 : OMNI ON, MONO
Mode 4 : OMNI OFF, MONO

○ : Yes
X : No

MODEL D-550 **MIDI Implementation Chart** (Separate CH)

*Recognized if key mode in patch function is 'Sep' or 'Sep-S'.

Function...	Transmitted	Recognized	Remarks
Basic Channel	Default Changed		1-16 1-16 Memorized
Mode	Default Messages Altered		Mode 3, 4 (M=1) X Memorized
Note Number	True Voice		0-127 12-108
Velocity	Note ON Note OFF		○ v=1-127 X
After Touch	Key's Ch's		X *
Pitch Bender			* 0-12 semi 9 bit resolution
Control Change	1		*
	5		*
	7		X
	6, 38		**
	64		*
Control Change	65		*
	100, 101		** (0) RPC (LSB, MSB)
Prog Change	True #		X
System Exclusive			X
System Common	Song Pos		X
	Song sel		X
	Tune		X
System Real Time	Clock		X
	Commands		X
Aux Message	Local ON/OFF		X
	All Notes OFF		○ (123)
	Active Sense		○
	Reset		X
Notes			* Can be set to ○ or X manually, and memorized. ** RPC=Registered parameter control number. RPC#0 : Pitch bend sensitivity Parameter values are given by Data Entry.

Mode 1 : OMNI ON, POLY
Mode 3 : OMNI OFF, POLY

Mode 2 : OMNI ON, MONO
Mode 4 : OMNI OFF, MONO

○ : Yes
X : No

8-16 VOICE LINEAR SYNTHESIZER MODULE
MODEL D-550

MIDI Implimentation

Date : Jun. 27. 1987
Version : 1.00

1. TRANSMITTED DATA

System Exclusive
Exclusive
Status
FOH : System Exclusive
7FH : BOX (End Of Exclusive)

Transmitted in the following two cases.
1) Operating Bulk-Dump
2) If Exclu of MIDI function is "P-Dump", this unit transmits all parameters in the patch when PATCH GROUP, PATCH BANK or PATCH NUMBER button is pressed.
Refer to Section 4, to see details.

2. RECOGNIZED RECEIVE DATA (MAIN CHANNEL)

Note Event
Note Off
Note On
Control Change
Modulation Depth (receive/ignore selectable)
Portamento Time (receive/ignore selection)
Data Entry MSB
Main Volume (receive/ignore selectable)
Tone Balance (receive/ignore selectable)
Data Entry LSB

Hold1 (receive/ignore selectable)
Portamento (receive/ignore selectable)
Chase
RPC LSB
RPC MSB
RPC MSB LSB Data Entry Description
RPC MSB LSB Data Entry Description

Program Change
Patch Change (receive/ignore selectable)
Channel After Touch
After Touch (receive/ignore selectable)
Pitch Bender Change
Pitch Bender (receive/ignore selectable)

Mode Message

All Note Off
OMNI OFF
OMNI ON
MONO
Control Change
Modulation (receive/ignore selectable)
Portamento (receive/ignore selectable)
Data Entry MSB
Data Entry LSB
Hold 1 (receive/ignore selectable)
Portamento (receive/ignore selectable)
RPC LSB
RPC MSB

Exclusive
Active Sensing

3. RECOGNIZED RECEIVE DATA (SEPARATE CHANNEL)

Note Event
Note Off
Note On
Control Change
Modulation (receive/ignore selectable)
Portamento (receive/ignore selectable)
Data Entry MSB
Data Entry LSB
Hold 1 (receive/ignore selectable)
Portamento (receive/ignore selectable)
RPC LSB
RPC MSB
RPC MSB LSB Data Entry Description

Channel After Touch

After Touch (receive/ignore selectable)
Pitch Bender Change
Pitch Bender (receive/ignore selectable)
Mode Message
All Note Off
Active Sensing

4. EXCLUSIVE COMMUNICATION

Address Description
Address Description
Address Description
Address Description

4.2 Partial Parameter

Table with columns: Offset Address, Description, and values. Lists parameters like WG PITCH COARSE, WG PITCH FINE, WG MOD LFO MODE, etc.

25H	0vvv vvvv	TVA BRAS POINT	(-50 +50) 0: 63.64-127 <A1->C7, >A1->C7	0: 175 7: 210 8: 250 9: 300 10: 350 11: 420 12: 500 13: 600 14: 700 15: 840	16H	0vvv vvvv	UPPER TONE KEY SHIFT	0-4R (-24 +24) 0-4R (-24 +24) 0-100 (-50 +50) 0-100 (-50 +50) 0-12 0-24 (-12 +12) 0-100 0-3 (1-4) 0-31 (1-32) 0-100 0-100 0-100 0-100 0: UL, 1: ULL, 2: ULUJ			
26H	0vvv vvvv	TVA BRAS LEVEL	0-12 (-12-0)	16: 8.4 17: 4.8 18: 5.7 19: 6.7 20: 8.0 21: 9.5 2: 0.3 1: 0.5 2: 0.7 3: 1.0 4: 1.4 5: 2.0 6: 3.0 7: 4.2 8: 6.0 0-24 (-12 +12)	17H	0vvv vvvv	LOWER TONE KEY SHIFT	0-4R (-24 +24) 0-4R (-24 +24) 0-100 (-50 +50) 0-100 (-50 +50) 0-12 0-24 (-12 +12) 0-100 0-3 (1-4) 0-31 (1-32) 0-100 0-100 0-100 0-100 0: BASIC CH, 1-16: CH1-16			
27H	0vvv vvvv	TVA ENV TIME 1	0-100	10: 1.4 11: 1.7 12: 2.0 13: 2.4 14: 2.8 15: 3.4 16: 4.0 17: 4.8 18: 5.7 19: 6.7 20: 8.0 21: 9.5	18H	0vvv vvvv	UPPER TONE FINE TUNE	0-100 (-50 +50) 0-100 (-50 +50) 0-12 0-24 (-12 +12) 0-100 0-3 (1-4) 0-31 (1-32) 0-100 0-100 0-100 0-100 0: UL, 1: ULL, 2: ULUJ			
28H	0vvv vvvv	TVA ENV TIME 2	0-100	22H	0vvv vvvv	CHASE MODE	0-100	23H	0vvv vvvv	CHASE LEVEL	0-100
29H	0vvv vvvv	TVA ENV TIME 3	0-100	23H	0vvv vvvv	CHASE TIME	0-100	24H	0vvv vvvv	CHASE TIME	0-100
2AH	0vvv vvvv	TVA ENV TIME 4	0-100	24H	0vvv vvvv	MIDI TRANSMIT CHANNEL	0: BASIC CH, 1-16: CH1-16	25H	0vvv vvvv	MIDI TRANSMIT CHANNEL	0: BASIC CH, 1-16: CH1-16
2BH	0vvv vvvv	TVA ENV TIME 5	0-100	25H	0vvv vvvv	MIDI SEPARATE RECEIVE CHANNEL	0: OFF 1-16: CH1-16	26H	0vvv vvvv	MIDI SEPARATE RECEIVE CHANNEL	0: OFF 1-16: CH1-16
2CH	0vvv vvvv	TVA ENV LEVEL 1	0-100	26H	0vvv vvvv	MIDI TRANSMIT PROGRAM CHANGE	0: OFF 1-100: NO1-100	27H	0vvv vvvv	MIDI TRANSMIT PROGRAM CHANGE	0: OFF 1-100: NO1-100
2DH	0vvv vvvv	TVA ENV LEVEL 2	0-100	27H	0vvv vvvv	CHASE SWITCH	0: OFF 1: ON	28H	0vvv vvvv	CHASE SWITCH	0: OFF 1: ON
2EH	0vvv vvvv	TVA ENV LEVEL 3	0-100	28H	0vvv vvvv	MAIN CH PORTAMENTO SWITCH	0: OFF 1: ON	29H	0vvv vvvv	MAIN CH PORTAMENTO SWITCH	0: OFF 1: ON
2FH	0vvv vvvv	TVA ENV SUSTAIN LEVEL	0-100	29H	0vvv vvvv	SEP CH PORTAMENTO SWITCH	0: OFF 1: ON	2AH	0vvv vvvv	SEP CH PORTAMENTO SWITCH	0: OFF 1: ON
30H	0vvv vvvv	TVA ENV END LEVEL	0: 0 1: 100	2BH	0vvv vvvv	EXTENSION	0-127	2BH	0vvv vvvv	EXTENSION	0-127
31H	0vvv vvvv	TVA ENV VELOCITY FOLLOW	0-4	2CH	0vvv vvvv	EXTENSION	0-127	2CH	0vvv vvvv	EXTENSION	0-127
32H	0vvv vvvv	TVA ENV TIME KEYFOLLOW	0-4	2DH	0vvv vvvv	EXTENSION	0-127	2DH	0vvv vvvv	EXTENSION	0-127
33H	0vvv vvvv	TVA MOD LFO SELECT	0: +LFO1 1: -LFO1 2: +LFO2 3: -LFO2 4: +LFO3 5: -LFO3	2EH	0vvv vvvv	EXTENSION	0-127	2EH	0vvv vvvv	EXTENSION	0-127
34H	0vvv vvvv	TVA MOD LFO DEPTH	0-100	2FH	0vvv vvvv	EXTENSION	0-127	2FH	0vvv vvvv	EXTENSION	0-127
35H	0vvv vvvv	TVA MOD AFTERTOUCH RANGE	0-14 (-7 +7)	30H	0vvv vvvv	EXTENSION	0-127	30H	0vvv vvvv	EXTENSION	0-127
36H	0vvv vvvv	EXTENSION	0-127	31H	0vvv vvvv	EXTENSION	0-127	31H	0vvv vvvv	EXTENSION	0-127
37H	0vvv vvvv	EXTENSION	0-127	32H	0vvv vvvv	EXTENSION	0-127	32H	0vvv vvvv	EXTENSION	0-127
38H	0vvv vvvv	EXTENSION	0-127	33H	0vvv vvvv	EXTENSION	0-127	33H	0vvv vvvv	EXTENSION	0-127
39H	0vvv vvvv	EXTENSION	0-127	34H	0vvv vvvv	EXTENSION	0-127	34H	0vvv vvvv	EXTENSION	0-127
3AH	0vvv vvvv	EXTENSION	0-127	35H	0vvv vvvv	EXTENSION	0-127	35H	0vvv vvvv	EXTENSION	0-127
3BH	0vvv vvvv	EXTENSION	0-127	36H	0vvv vvvv	EXTENSION	0-127	36H	0vvv vvvv	EXTENSION	0-127
3CH	0vvv vvvv	EXTENSION	0-127	37H	0vvv vvvv	EXTENSION	0-127	37H	0vvv vvvv	EXTENSION	0-127
3DH	0vvv vvvv	EXTENSION	0-127	38H	0vvv vvvv	EXTENSION	0-127	38H	0vvv vvvv	EXTENSION	0-127
3EH	0vvv vvvv	EXTENSION	0-127	39H	0vvv vvvv	EXTENSION	0-127	39H	0vvv vvvv	EXTENSION	0-127
3FH	0vvv vvvv	EXTENSION	0-127	3AH	0vvv vvvv	EXTENSION	0-127	3AH	0vvv vvvv	EXTENSION	0-127

4.3 Common Parameter

Offset Address	Description	
00H	0vvv vvvv	0-63
09H	0vvv vvvv	0-63
0AH	0vvv vvvv	0-6
0BH	0vvv vvvv	0-2
0CH	0vvv vvvv	0-4
0DH	0vvv vvvv	0-50
0EH	0vvv vvvv	0-50
0FH	0vvv vvvv	0-50
10H	0vvv vvvv	0-50
11H	0vvv vvvv	0-100
12H	0vvv vvvv	0-100
13H	0vvv vvvv	0-100
14H	0vvv vvvv	0-100
15H	0vvv vvvv	0-100
16H	0vvv vvvv	0-100
17H	0vvv vvvv	0-100
18H	0vvv vvvv	0-100
19H	0vvv vvvv	0: TRI 1: SAW 2: SQU 3: RND

4.4 Patch Parameter

Offset Address	Description	
00H	0vvv vvvv	0-63
11H	0vvv vvvv	0-63
12H	0vvv vvvv	0: WHOLE 1: DUAL 2: SPLIT 3: SEPARATE 4: WHOLE-S 5: DUAL-S 6: SPLIT-US 7: SPLIT-LS 8: SEPARATE-S
13H	0vvv vvvv	0-60 (C2,C#2-C7)
14H	0vvv vvvv	0: UPPER 1: LOWER 2: UPPER/ LOWER
15H	0vvv vvvv	0: UPPER 1: LOWER 2: UPPER/ LOWER

4.5 Reverb Block

Offset Address	Description	
00 00H	0000 aaaa	REVERB DATA 1
00 01H	0000 bbbb	aaaa bbbb
00 02H	0000 aaaa	REVERB DATA 2
00 03H	0000 bbbb	aaaa bbbb
02 76H	0000 aaaa	REVERB DATA 188
02 77H	0000 bbbb	aaaa bbbb

4.6 System area

Offset Address	Description	
00H	0000 0000	PATCH MEMORY WRITE
01H	0000 0000	

Temporary area data will be written in the patch memory which had been selected before editing. If a card patch had been selected, PATCH MEMORY WRITE will be ignored.

5. TRANSMITTED EXCLUSIVE MESSAGES IN NORMAL MODE

5.1 Data set (One Way) DT1 12H

Transmitted in the following two cases.

- When Request Data (RQ1) is recognized, Data set is transmitted on the channel set with Basic CH of MIDI func., regardless of the transmit channel set in the patch. The size of the Data set is according to the address size specified by Request Data (RQ1).
- When any one of Patch group, bank, number button is pressed, all data in the Temporary area (all parameters of selected patch and tones) is transmitted if Exclu of MIDI Function is set "P-Dump". In this case, it is transmitted on the transmit channel set in the patch.

6. RECOGNIZED EXCLUSIVE MESSAGES IN NORMAL MODE

6.1 Request Data (One way) RQ1 11H

Recognized if Exclu in the MIDI function is ON or P-Dump.

6.2 Data set (One Way) DT1 12H

Recognized if Exclu in the MIDI function is ON or P-Dump.

7. TRANSMITTED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE

Transmitted on the channel set with Basic CH of MIDI Function, regardless of the transmit channel set in the patch.

Address of first Data set command (DT1), Want to send data (WSD) or Request data (RQD) is [02-00-00] (top of memory area)

7.1 One way transfer

7.1.1 Data set DT1 12H

Transmitted when "Enter" button is pressed in "Bulk Dump, 0".

7.2 Handshaking Communication

7.2.1 Want to send data WSD 40H

Transmitted when "ENTER" button is pressed in "Bulk Dump" mode.

7.2.2 Request Data RQD 41H

Transmitted when "ENTER" button is pressed in "Bulk Load" mode.

8. RECOGNIZED EXCLUSIVE MESSAGES IN DATA TRANSFER MODE

If the assigned address exceeds Memory area, it is ignored. The size that exceeds Memory area should not be assigned.

8.1 One Way Transfer

8.1.1 Data set DT1 12H

8.2 Handshaking Communication

8.2.1 Want to send data WSD 40H

8.2.2 Request Data ROD 41H

8.2.3 Data set DAT 42H

8.2.4 Acknowledge ACK 43H

8.2.5 End of Data EOD 45H

8.2.6 Communication Error ERR 4EH

8.2.7 Rejection RJC 4FH

Address Map

