MODEL 400 DRUMTRAKS

PRELIMINARY SERVICE DATA

Contents

Manual No: TN400-0
Issued: December, 1983

THEORY OF OPERATION

The following discussions are keyed to the schematic pages.

SHEET A PCB 1 CONTROL PANEL SD400-1A

LED Matrix

The LED matrix is standard. U102/3 are driver latches clocked by -OLEDS from the I/O decoder. Latched bits turn on the buffer transistors, pulling the LED anodes high. The LED cathodes are pulled low by sink U104. U105 is an eight-bit addressable latch. The high DATA input is routed to one of the outputs, as selected by the address inputs and clocked by -OSINK (also from the I/O decoder).

Switch Matrix

-OSINK also clocks U107, which drives the switch matrix. Buss driver U106 places bits encoded by closed switches on to the data buss. The clock -ISWI is gated by U213-8 when -IORD and A6 are low.

Multiplexer

A two-in/one-out multiplexer for the PER INSTRUMENT VOLUME and TUNING knobs is shown at the lower left. The POT SEL bit which switches between the two wipers comes from the miscellaneous output latch. The wiper voltage, Vmux, controls the frequency of voltage-controlled oscillator U221.

Metronome/Master Volume

On the right is shown the metronome volume control. The width of the METRO pulse is fixed by the metronome one-shot. When METRO is low, U101-15 is grounded (by pin 2). So the metronome is off. METACC, from trigger latch 2, is normally low, so the metronome pulse flows through the 10K resistor on its way through the volume control and to the audio summer. To accent the metronome (which occurs on the first beat of the pattern), METACC goes high, bypassing the resistor.

The MASTER VOLUME pot divides the output of the audio summer, and sends this to the output amplifier.

SHEET B PCB 2 CPU SD400-2A, 1/4

SYSTEM CLOCK

The system clock is generated by Y201 8-MHz crystal and two inverters of U212 wired as a simple RC oscillator. The 4-MHz output of divider U221 clocks the CPU. The 2-MHz output clocks two of the three-section timer U211. (The third section is in the ADC, shown at the right of the page.)

The first section, U211-10, drives the tempo counter with 4.8 kHz. When gated, the tempo counter increments at this rate to the count with which it has been programmed, then issues SCLK. After some miscellaneous logic (elaborated below), this signal interrupts the CPU, forcing it into its output routine.

2-MHz also clocks the third 8253 section, U211-17--at the right of the page. To accomplish ADC, this counter accumulates a number of 2-MHz pulses which occur while it is gated on by the ADC VCO. (See also below.)

The 500-kHz clock drives the UART, U202, which divides it internally to the MIDI clock rate of 31.25 kBaud. It also clocks the non-maskable interrupt (NMI) flip-flop (FF), as discussed below.

CPU

With the clock running and -RESET high, the CPU's program counter is initialized to memory address 0000H (Hex). All address lines A0-A15 will be low. A0 through A12 define the first memory location in EPROM U206. But this is not enough to read the instruction in this location because many memory and I/O devices share these address lines. A signal is needed to differentiate the EPROM from the RAMs and other devices. This signal is generated by U215 Memory Address Decoder. With A11 through A13 low, A15 low, -MREQ low--which indicates that the address bus holds a valid memory address--the decoder output -Y0 goes low. -RFSH indicates that the address bus holds a valid refresh address. Applied to G1, this signal is used to disable the decoder whenever this is the case. The -Y0 output makes U282-3 low, and clocks (-OE) the output of the EPROM. (Although using the 2764 -CE input would reduce power consumption, -OE was used for maximum memory access speed.) The EPROM places the instruction from location 0 on the data bus (D0-D7), from which it is retrieved by the CPU's instruction register.

Outputs -Y0 through -Y3 each decode 2K bytes of memory. All EPROM operations are memory-read. When the CPU needs to write to or read one of the non-volatile RAMs, the decoder selects -R1-4. These strobes are gated to the RAMs by the four sections of U203 only if -PWR ON is low. The transfer of data from CPU to RAM is enabled by the -WR (write) line being true. The opposite direction, from RAM to CPU, is enabled by -RD (read).

The uppermost memory-mapped device is U202 UART, which has two control registers that need to be accessed. These are decoded somewhat differently from the other memory locations. The combination of A0, A13, A14, A15 define the read and write addresses. The RC-delay provided to -RD through U213-11 times the EUART clock pulse needed to interface this 6800-system part to the Z-80A.

Input/output interface follows similar principles as memory interface. The address lines define ports which are validated by -IORQ (instead of -MREQ). -IORQ (CPU pin 20) connects to an I/O decoder which is similar to the memory decoder. With regard to I/O, -RD true defines an input operation, typically from data bus drivers which hold data from the control panel. -WR defines an output to a latch or register. For example the timer is I/O mapped because it is too slow to run memory-mapped at this speed. (I/O automatically inserts an extra 250 ns wait state.)

COMPUTER TROUBLESHOOTING

For troubleshooting, it should be emphasized that most computer malfunctions are caused either by failures in the Clock or Power On/Reset circuits, or by failures of devices connected to the data bus. A shorted latch input (for instance) can prevent an entire data line from achieving the minimum voltage needed to signify a high signal. Shorts between data lines will also confuse the computer terribly.

If you suspect a data bus problem, try to pick out the lines with questionable levels. On a normal data bus the low voltages don't rise above 500 mV, while the high voltages are generally 4 to 5V. Malfunctions are indicated especially by signals in the 1- to 3-V range and by the lack of solid ground.

Shorts may occur within a device or between printed traces. But since the computer is known to have been running, the problem is more likely to be device failure than a problem with the traces. Nevertheless it is probably best to begin troubleshooting the computer with a close visual inspection, especially around sockets. (Magnifying glasses are often helpful.) If you see no evidence of mechanical problems such as broken traces, broken sockets, conductive particles, botched soldering or careless repair attempts, try removing or swapping socketed devices such as the CPU, EPROM, and RAM. Even if the computer isn't running (due to one of these devices being missing), a change in static voltage indications could be a good clue about which is the bad part.

If you have checked all socketed components (perhaps even a few unsocketed ones), and tried to find the problem with a 'low-ohms' meter, then there may be no recourse but to cut printed circuit traces. The customary technique is to make the first cut at the electrical center of a the bus line, to isolate the problem to one half or the other. When the cut has yielded information on the direction of the malfunction, it should immediately be repaired--to prevent unrelated malfunctions. Then halve the suspect trace again, and so on, until the bad IC (or socket, or shorted trace) is isolated.

INTERRUPTS

With the basic architecture of the microcomputer now introduced, we can look at the input and output processes in more detail.

To accomplish real-time tasks such as playing the instruments and responding to MIDI inputs, the Drumtraks microcomputer is interrupt-driven at a constant rate. The Z-80 has two interrupt inputs: -INT (Maskable Interrupt) and -NMI (Non-Maskable Interrupt). -INT is constantly clocked by the tempo counter. -NMI is used only for MIDI (see below).

Timer U211-10 which forms the interrupt clock was briefly mentioned above. This third of the triple-timer device is programmed to yield a 4.8-kHz output. The tempo divider is programmed with a terminal count specific to the selcted tempo. In other words, as the /TEMPO divider value changes, the interrupt rate changes. When EXTCLK from U216 miscellaneous output latch goes high, SCLK goes low on the first 4.8-kHz input pulse. U223-3 is high, so U223-11 is low. -INT is high. Flip-flop U222-1 is automatically reset when both -M1 and -IORQ go low. When the tempo count is reached, SCLK goes high. U223-3 goes low. U223-11 goes high, clocking -Q, -INT true. If an external clock has been detected by comparator U220, CCIN will be high, so U223-4 goes low, producing the interrupt (if enabled).

Because this interrupt is "maskable," there are some rare occasions during which -INT is ignored. But normally each interrupt pulse forces the CPU to record or transmit any data synchronized to that clock pulse. In the "background period" between the end of the interrupt routine and the next interrupt, the CPU:

Refreshes all CV Sample/Holds.
Refreshes the trigger latches, as required.
Refreshes the LEDs.
Reads the ADC.
Reads the control panel.

MIDI

U202 MIDI UART allows two microcomputers to communicate pattern, song, and program information. As the pattern plays this data is converted to the MIDI protocol and sent to the UART one byte at a time, for transmission to any receiver which may be connected. The MIDI standard hardware is a 5-mA current loop, designed especially to prevent the formation of audio ground loops which can develop in complex systems.

The UART converts parallel bytes written to its memory-mapped transmit register into serially-formatted bytes consisting of a start bit, 8 data bits (D0 to D7), and a stop bit. The transmission occurs at 31.25 kBaud, which is obtained by internally dividing the 500 kHz TxC (and RxC) input by 16. Transmitter data out is buffered by U201-11, which can sink up to 16 mA. If transmit data is low, current flows from +5V through R230, over pin 4 of both connectors, through R231 and optoisolator LED U283, and returns over connector pins 5. D203 protects the receiver from reverse-polarity spikes. The output of the optoisolator is normally pulled high by R229. But with the LED on, the isolater switch turns on, sending a low to the UART receiver input. Notice that while the MIDI OUT jack is grounded to the chassis, MIDI IN is not. This allows the cables to provide their shielding services without creating ground loops.

When the UART has not received data, its pin 7 -NMIREQ is high. Each 500-kHz clock pulse on NMI FF U222-13 clocks this signal, -NMI false, to the CPU, where it has no effect. But when a complete serial byte is received, -NMIREQ goes low, indicating the receive register is holding data. This data needs to be retrieved, so that the next byte of real-time data can be received. -NMI is now true and it will take at most 2 us to be clocked through the NMI FF. When it sees the negative edge on its pin 17, the CPU completes its current instruction, makes a note to itself where it was in the program, then branches to the routine which handles the UART input.

After the data is handled, the CPU prepares for the next MIDI interrupt by clearing the NMI FF with the -NMI CLR pulse from the miscellaneous output latch.

I/O

Returning to the I/O decoder U214 (lower left), the active output -Y0 to -Y7 is selected by A2-4 when A7 is high, -IORQ is low, and M1 is high (U2112-12 low). -OCNTR selects the timer U211, which was discussed above.

-OSHMUX selects latch U215, which outputs the sample/hold strobe bits and the external metronome pulse.

-OMISC clocks miscellaneous output latch U216. The -EXTCLK bit, POT SEL, and NMI CLR bits have been discussed. In addition, U212-6 provides the clock/cassette output signal to those two jacks. POTADC enables ADC VCO U221. This ADC works by period measurement. When Vmux is low, the pulse at U221-5 will be wider than when Vmux is high. Therefore the number of 2-MHz pulses counted by U211-17 will be proportionately higher than if Vmux is high. Finally, the MET bit triggers metronome one-shot U225 to produce the metronome pulse. This goes to the METRONOME VOLUME control on the front panel.

-OTRIGA clocks U217 trigger latch A, producing the trigger pulses which start each channel clock to read their respective ROMs.

-0TRIB clocks U219 trigger latch B, which provides additional signals for selecting between instruments in certain channels, as well as the MET ACC signal to the metronome volume control.

-ODAC, -OSINK, and -OLEDS have already been discussed.

Miscellaneous input driver U224 is clocked by -IMISC, which appears from U213-6 when -IORD and A5 are low. It accepts the cassette and two footswitch inputs.

SHEET C PCB 2 SAMPLE/HOLDS, SD400-2A, 2/4 POWER SUPPLY

DAC, DEMULTIPLEXER, SAMPLE/HOLDS

U226 is an eight-bit digital-to-analog converter (DAC) used to generate control voltages (CVs) for the channel volumes and tuning. Follower U230-7 creates a -5-V reference. -ODAC from the I/O decoder clocks latches data for the DAC. U230-1 converts the DAC output current to the range 0-5V.

U232 and U228 distribute Vdac sequentially to the sample/holds, according to the state of the S/H ABC and I inputs from the sample/hold control latch. Address lines ABC select one of eight outputs on both devices. But only one device is enabled at a time, by I1 or I2 going low.

Oweing to the very high input impedance of the 084s, each sample/hold capacitor holds its specific Vdac charge while the others are being refreshed. The six volume CVs (U228) go to each channel DAC.

U232 demultiplexes the tuning CVs. For all channels, these voltages adjust the frequency of a voltage-controlled clock. These VCOs ultimately clock the drum sounds out of their ROMs. The lower the voltage, the higher the clock frequency. The higher the clock frequency, the higher the tuning. For the lower-frequency channels 1 (BASS) and 3 (TOMS) the tuning CV is also tapped to control the cutoff frequency of the channel voltage-controlled filter (VCF).

POWER SUPPLY

The high-voltage transformer secondary drives a bridge rectifier for the +/- 15V supplies. The low-voltage winding is full-wave rectified to two 5-V regulators and the power detect circuitry. The Vnv battery supplies 2.9V, which D205 drops to 2.2V. This is sufficient to hold the non-volatile memory. When power is switched on, U301 through D204 overrides Vnv, providing standard operating voltage for the NV RAMs. D304 biases the common terminal of the regulator 0.6V above ground. This sets an output of +5.6V. But D204 drops this back to +5V. D205 prevents the regulator voltage from charging the (non-rechargable) lithium battery.

U204 in the power detect circuit is powered by Vnv. U204-4 is high because both inputs are low (since power is off). This high is applied directly to U204-9, and to U204-8 through the diode. U204-10 -RESET is therefore low (true). The CPU will remain reset until this line goes high (false). Inverting -RESET, U204-11 is high. In other words, -PWR ON is also false. This disables RAM access.

When power is switched on, the first peak in the low-voltage supply appears across divider R268/R269. When the divided voltage exceeds the CMOS high threshold of 3.5V, U204-4 goes low. Input U204-9 goes low immediately. Pin 8, however, is held high by the (Vnv) charge on C251, which begins to discharge through R270. After about one second, pin 8 falls low enough so U204-10, -RESET can go high, enabling the CPU. -PWR ON goes low, enabling RAM access.

AUDIO OUTPUT

U275-1 sums the six channel outputs and metronome, and sends the mixture to the MASTER VOLUME knob. It returns to amplifier U275-7, which drives the output jack.

SHEET D PCB 2 CHANNELS 1-3 SD400-2A, 3/4

The percussion sounds are created by clocking eight-bit numbers out of ROM, and converting them to analog values which trace-out the instrument waveforms. In some channels this basic process is supplemented with voltage-controlled analog filtering.

CHANNEL 2

We begin with channel 2 because it is the simplest. The snare and rim are two very short sounds. Therefore both can fit into ROM U244. They are selected by RT2, which controls the most-significant (MS) address bit.

When TR2 appears, flip-flop U246-13 and twelve-bit counter U245 are cleared. This sets the counter address to the first value of the waveform for the selected instrument. With Q low, U251-11 gates through voltage-controlled channel clock to increment the counter. The clock rate determines the instrument tuning. As the waveform is clocked, DAC U243 modulates the programmed VOL 2 CV. U242-1 converts the DAC current output to a voltage which is buffered by U242-7. The output is ac-coupled to the channel jack, and summed into the audio mixer.

When the instrument has been clocked out, CD11 goes high and U250-15 goes low. This forces Q high, disabling the clock input to the counter.

CHANNEL 1
In channel 1 the basic voice is supplemented by a low-pass filter with its own envelope generator. The basic operating range of the filter is controlled by the same CV which controls the channel clock rate. Thus the filter follows the instrument tuning.

The envelope generator is triggered when CD6 goes high. U240-2 goes high, turning on Q201. The envelope decay is produced by the discharge curve of C267.

CHANNEL 3
Channel 3 functions similarly to channel 1.

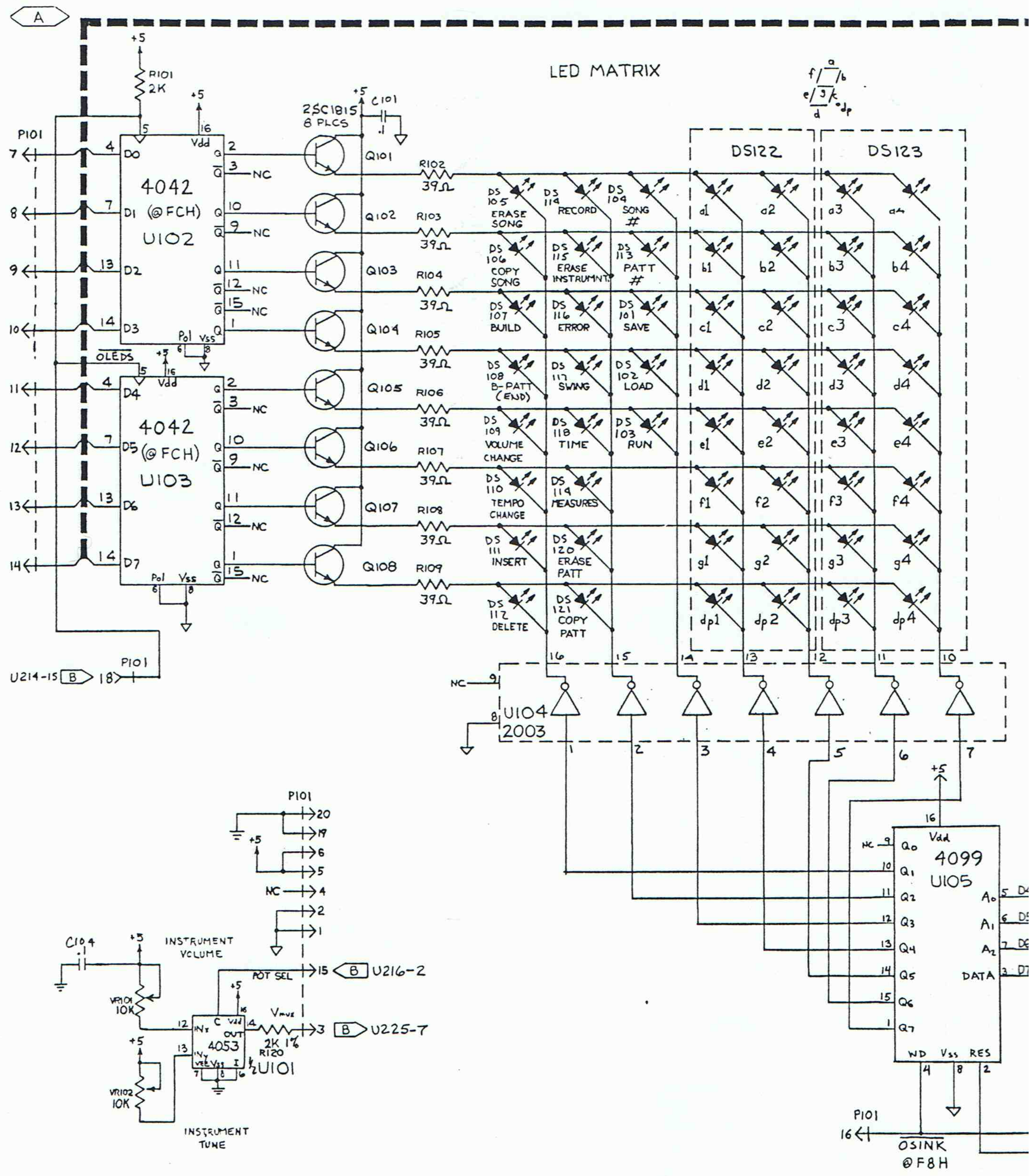
SHEET E PCB 2 CHANNELS 4-6 SD400-2A, 4/4

CHANNEL 6
Channel 6 is similar to channel 1. RT6A selects one instrument in both ROMs, while RT6B selects the ROM read.

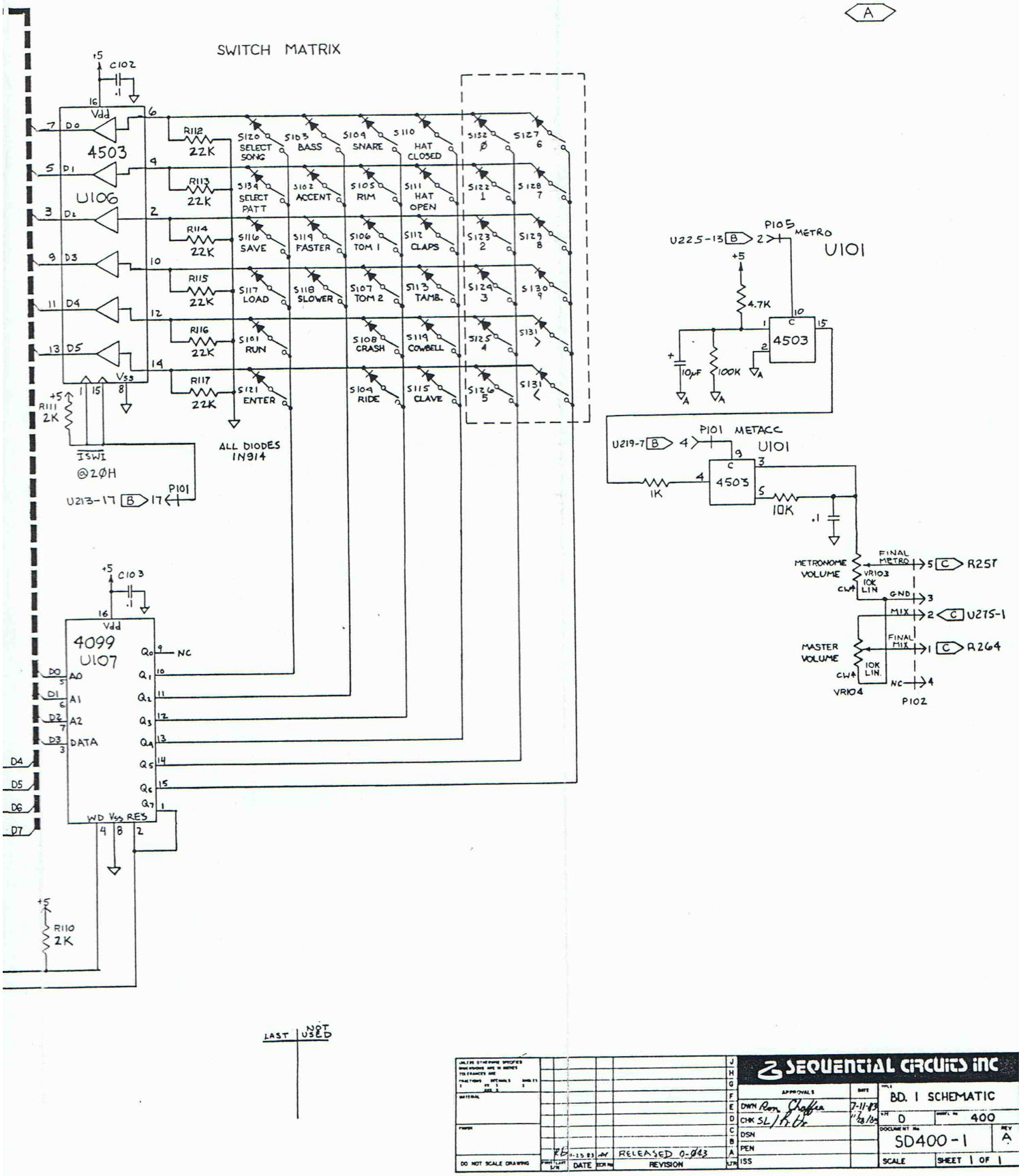
CHANNEL 4
The cymbal channel contains the longest sounds, requiring four ROMs to be read successively for each instrument. RT4 selects the instrument. Each time the twelve-bit counter wraps around, the CD12 pulse is clocked down the shift register made from U272/73. The register outputs enable the ROMs.

CHANNEL 5
The hi-hat channel supplements the channel 1 configuration with a T flip-flop, U285-13, which divides the CLOCK 5 frequency by two.

The VOL 5 CV receives some processing which introduces more realistic dynamics. When TR5 goes high, U269-2 goes low. Q203 is off and VOL 5 flows through D208 and U276-1. When CD6 goes high, U270-12 goes low. U281-11 goes high, which clocks the flip-flop low over to Q, and high over to -Q. This turns on Q203 to pull-down the volume (at the close of the open hi-hat). This control is also enabled by RT5, for the closed hi-hat. When the instrument has played, -Q of END flip-flop U269(-12) goes low. This shuts off volume by pulling it down through the diode.



A
LED MATRIX
R101 2K
+5
P101
4042 (@FCH) U102
4042 (@FCH) U103
2SC1815 8 PLCS
C101 .1
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
R102 39Ω
R103 39Ω
R104 39Ω
R105 39Ω
R106 39Ω
R107 39Ω
R108 39Ω
R109 39Ω
OLEDS
NC
DS122
DS123
DS 105 ERASE SONG
DS 114 RECORD
DS 104 SONG #
DS 106 COPY SONG
DS 115 ERASE INSTRUMNT
DS 113 PATT #
DS 107 BUILD
DS 116 ERROR
DS 101 SAVE
DS 108 B-PATT (END)
DS 117 SWING
DS 102 LOAD
DS 109 VOLUME CHANGE
DS 118 TIME
DS 103 RUN
DS 110 TEMPO CHANGE
DS 119 MEASURES
DS 111 INSERT
DS 120 ERASE PATT
DS 112 DELETE
DS 121 COPY PATT
U104 2003
U214-15 B 18
4099 U105
P101 16 OSINK @F8H
C104 .1
INSTRUMENT VOLUME
VR101 10K
POT SEL
15 B U216-2
4053 U101
Vmus
2K 1% R120
3 B U225-7
VR102 10K
INSTRUMENT TUNE



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FINISH						D	CHK SL/R.Ch 7/28/83
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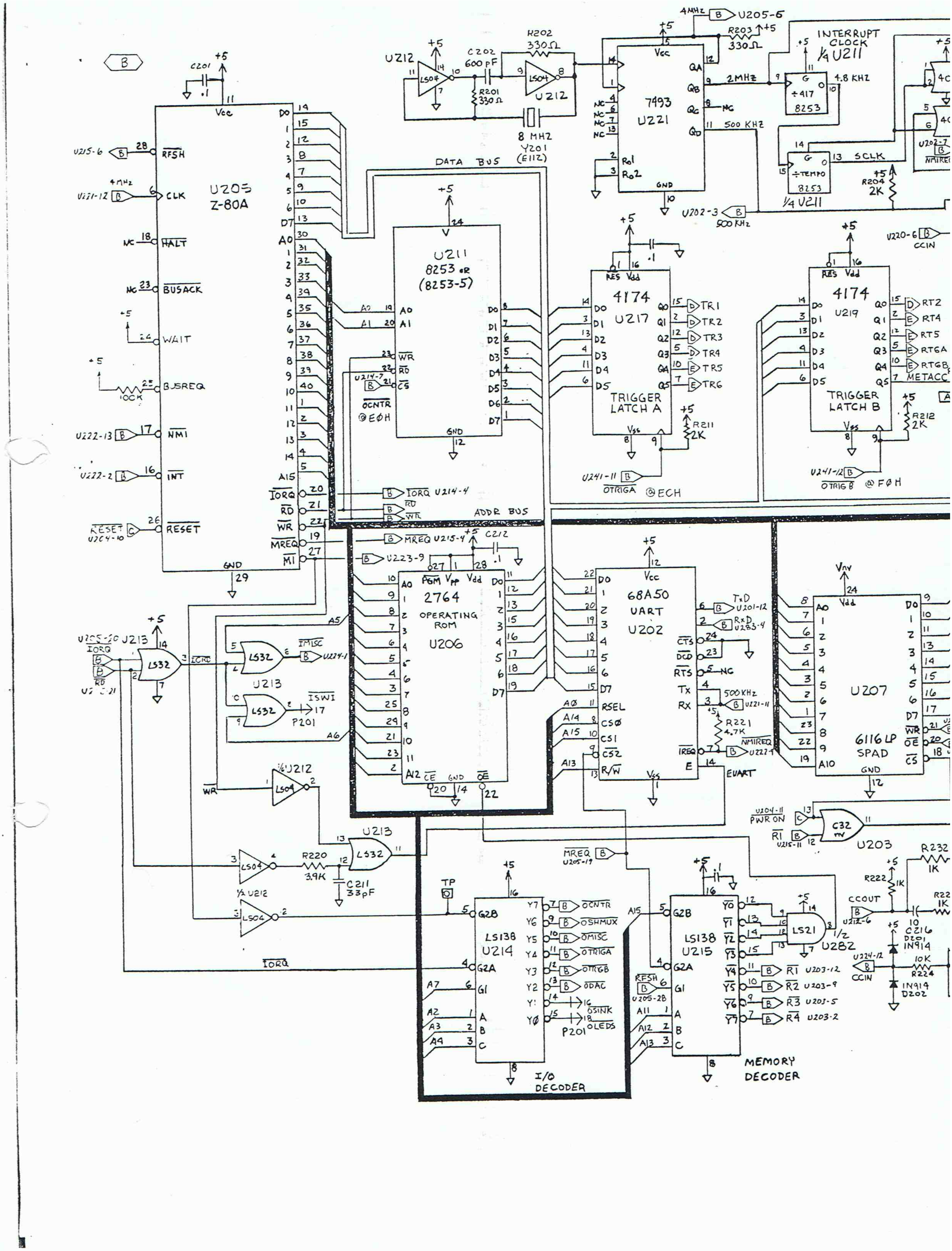
SHEET 1 OF 1



B
U205
Z-80A
DATA BUS
ADDR BUS
U211
8253 or (8253-5)
8 MHZ
Y201
(E112)
7493
U221
INTERRUPT CLOCK
1/4 U211
8253
SCLK
÷TEMPO
4174
U217
TRIGGER LATCH A
4174
U219
TRIGGER LATCH B
2764
OPERATING ROM
U206
68A50
UART
U202
U207
6116 LP
SPAD
LS138
U214
I/O DECODER
LS138
U215
MEMORY DECODER
U213
U203
R220
3.9K
C211
33pF
R221
4.7K
R211
2K
R212
2K
R204
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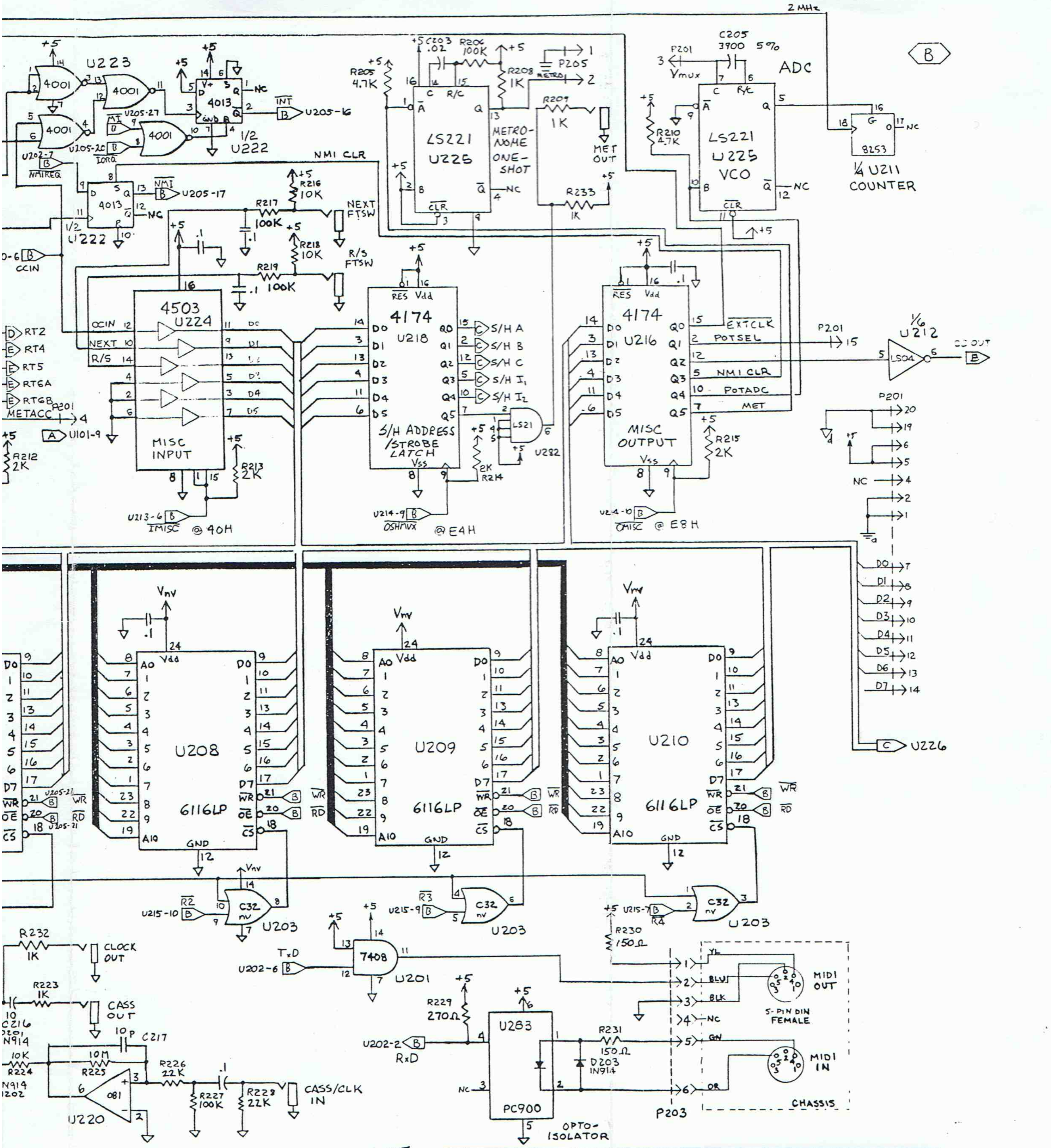
R202
330Ω
R203
330Ω
R201
330Ω
C202
600 pF



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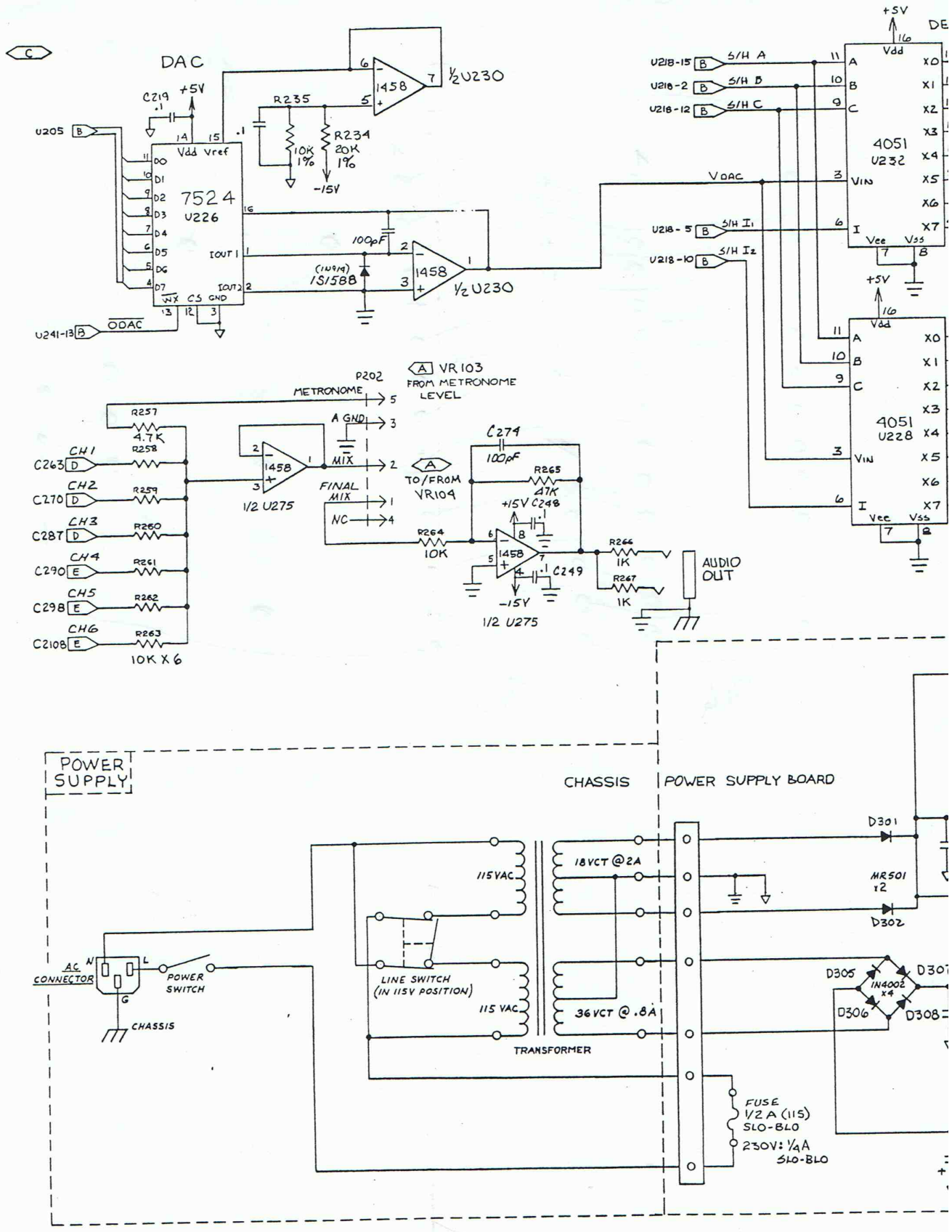
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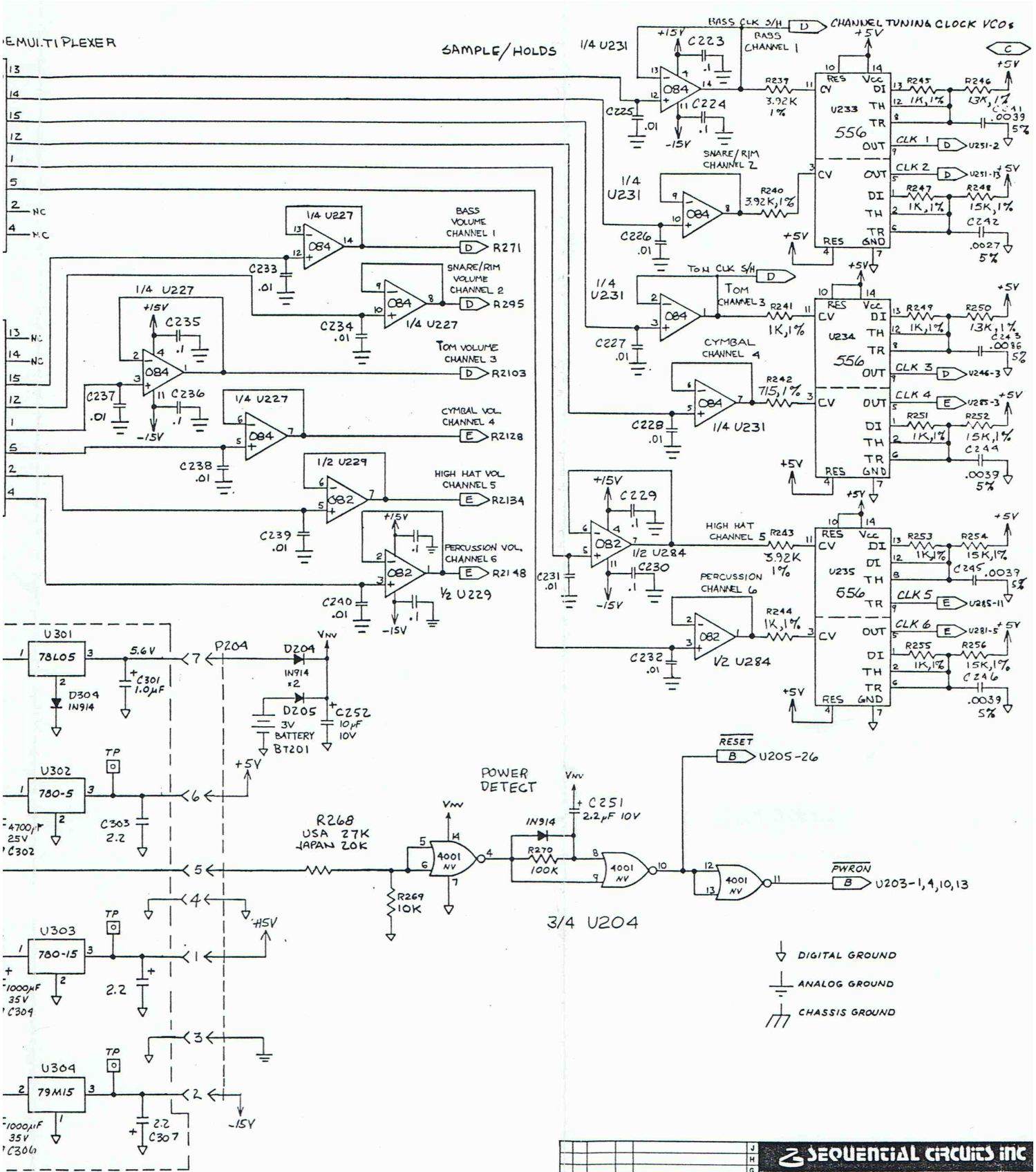
DAC
C219
.1
+5V
U205
B
Vdd Vref
7524
U226
D0
D1
D2
D3
D4
D5
D6
D7
WR
CS
GND
IOUT1
IOUT2
R235
10K 1%
R234
20K 1%
-15V
1458
1/2 U230
100pF
(1N914)
1S1588
1/2 U230
U241-13
B
ODAC
+5V
Vdd
16
U218-15
B
S/H A
U218-2
B
S/H B
U218-12
B
S/H C
4051
U232
A
B
C
VIN
X0
X1
X2
X3
X4
X5
X6
X7
Vee
Vss
VDAC
U218-5
B
S/H I1
U218-10
B
S/H I2
4051
U228
P202
METRONOME
5
A
VR103
FROM METRONOME LEVEL
R257
4.7K
R258
CH1
C263
D
CH2
C270
R259
D
CH3
C287
R260
D
CH4
C290
R261
E
CH5
C298
R262
E
CH6
C2108
R263
E
10K X 6
A GND
MIX
FINAL MIX
NC
1458
1/2 U275
A
TO/FROM VR104
C274
100pF
R265
47K
+15V
C248
R264
10K
1458
C249
-15V
1/2 U275
R266
1K
R267
1K
AUDIO OUT
POWER SUPPLY
CHASSIS
POWER SUPPLY BOARD
AC CONNECTOR
N
L
G
POWER SWITCH
CHASSIS
115VAC
LINE SWITCH (IN 115V POSITION)
115 VAC
18VCT @2A
36VCT @ .8A
TRANSFORMER
D301
MR501 x2
D302
D305
D306
IN4002 x4
D307
D308
FUSE
1/2 A (115) SLO-BLO
230V: 1/4A SLO-BLO



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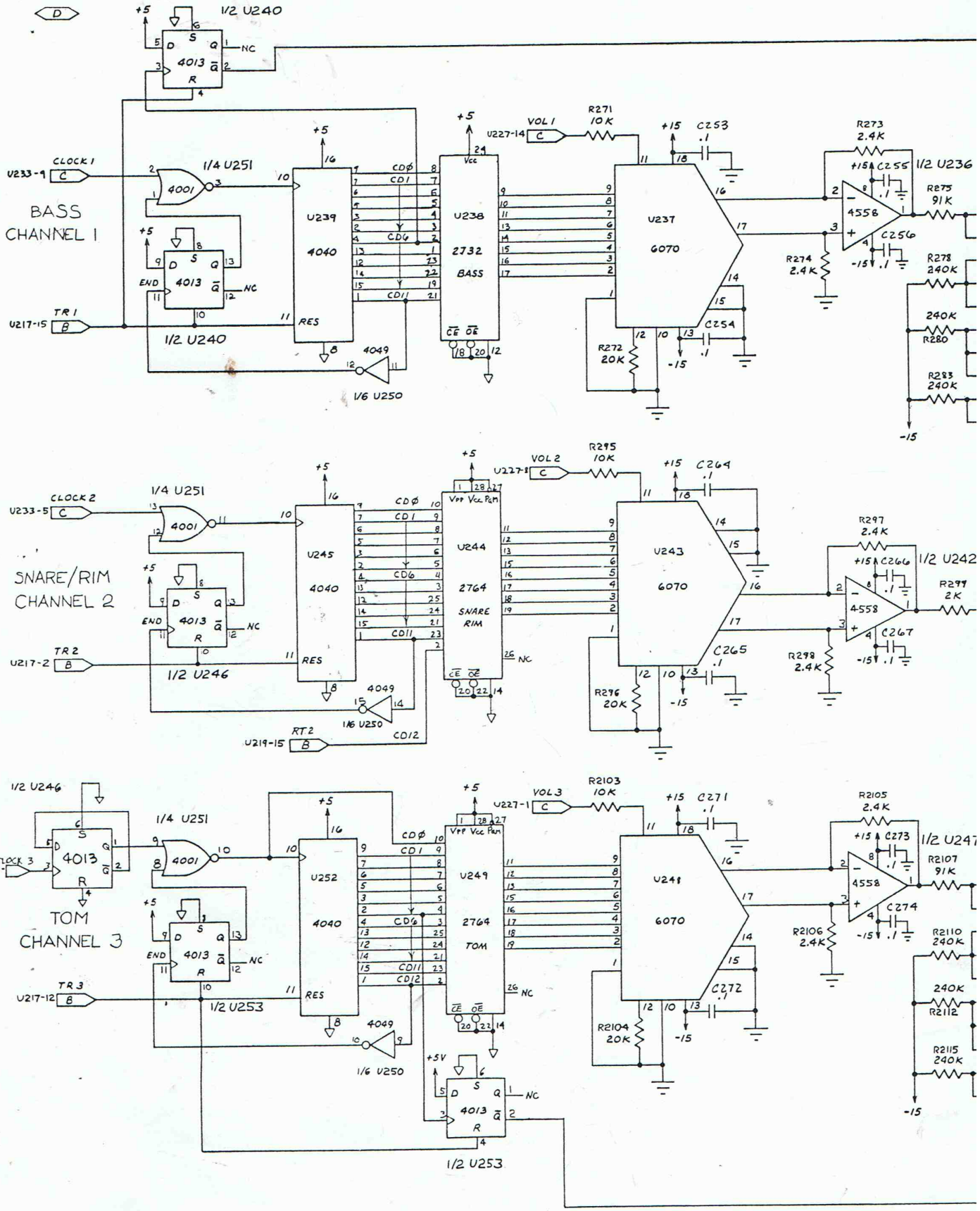
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BASS
CHANNEL 1
CLOCK 1
U233-9
1/4 U251
4001
U239
4040
U238
2732
BASS
U237
6070
VOL 1
U227-14
R271
10K
C253
.1
R273
2.4K
1/2 U236
4558
C255
C256
R275
91K
R274
2.4K
R278
240K
240K
R280
R283
240K
-15
TR 1
U217-15
1/2 U240
4049
1/6 U250
R272
20K
C254
SNARE/RIM
CHANNEL 2
CLOCK 2
U233-5
1/4 U251
U245
4040
U244
2764
SNARE
RIM
U243
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VOL 2
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R295
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.1
R297
2.4K
1/2 U242
C266
C267
C265
R299
2K
R298
2.4K
R296
20K
TR 2
U217-2
1/2 U246
RT 2
U219-15
CD12
TOM
CHANNEL 3
CLOCK 3
U234-3
1/2 U246
1/4 U251
U252
4040
U249
2764
TOM
U241
6070
VOL 3
U227-1
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C271
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R2105
2.4K
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C273
C274
R2107
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R2106
2.4K
R2110
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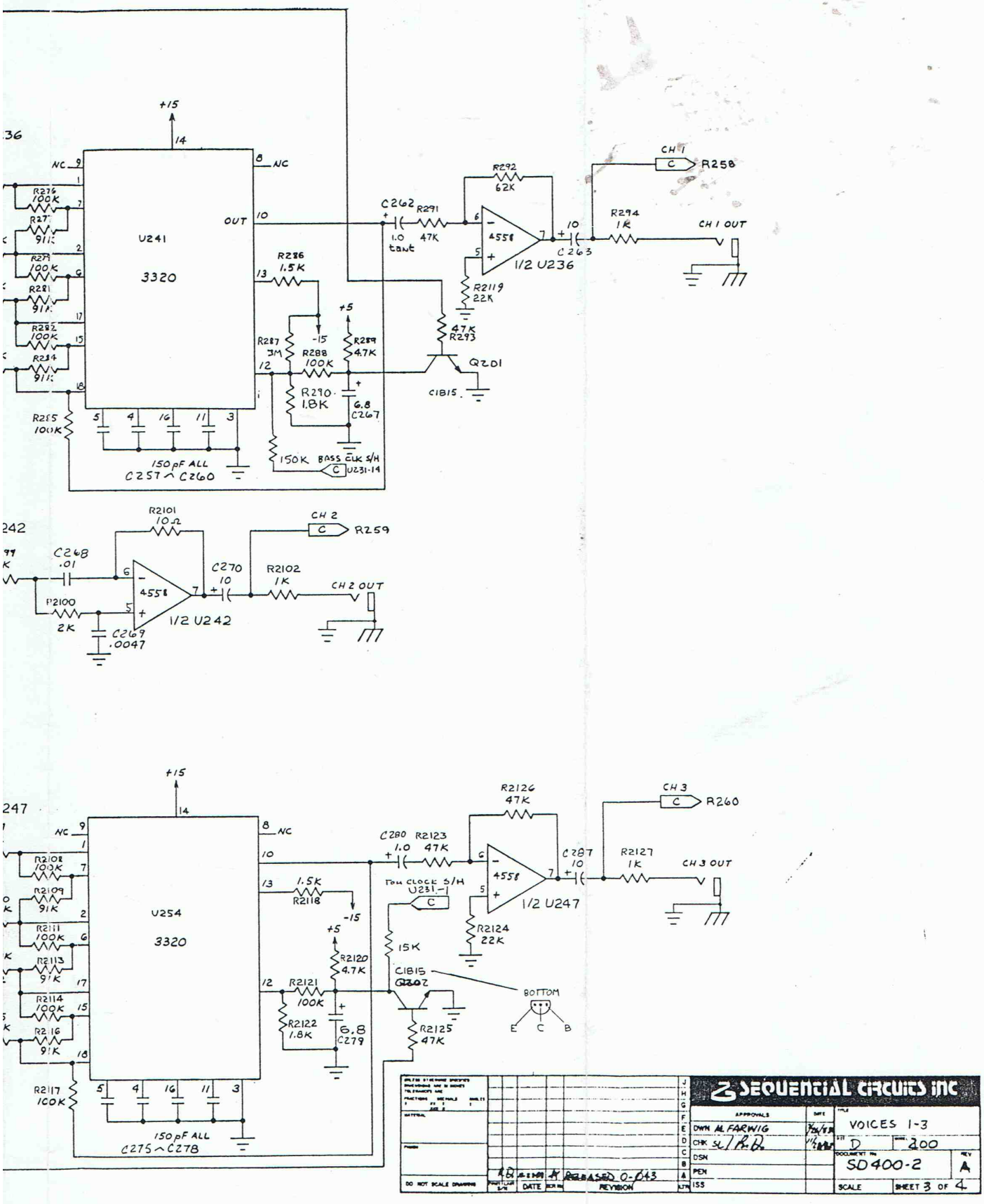
1/2 U253



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								C	
								B	
								A	

DO NOT SCALE DRAWING

RELEASED 0-043

DATE | REVISION

SEQUENTIAL CIRCUITS INC

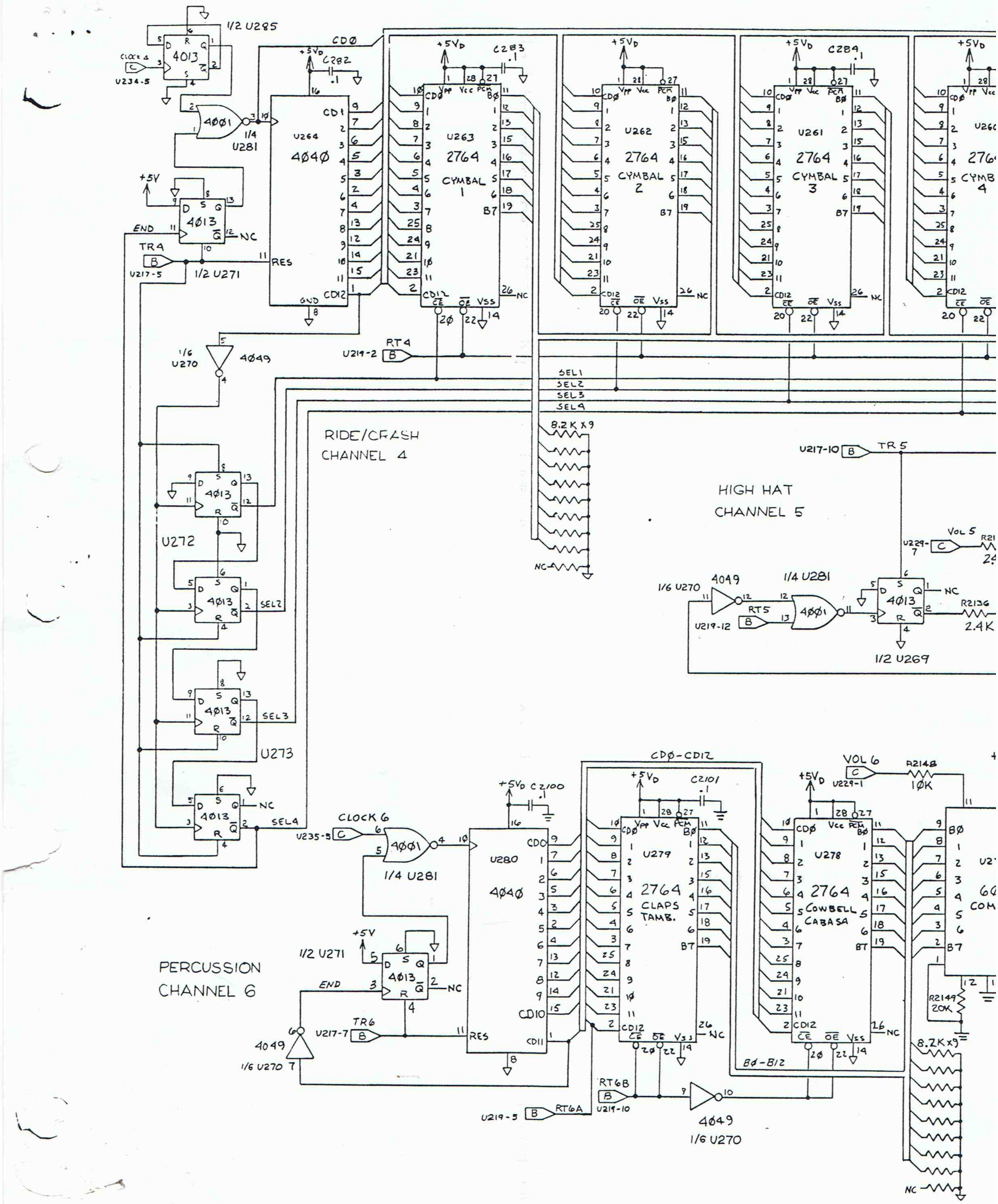
APPROVALS	DATE
DWN M. FARWIG	7/14/83
CHK [illegible]	7/14/83
DSN	
PEN	
ISS	

TITLE: VOICES 1-3

SIZE: D | DWG. NO. 200

DOCUMENT NO. SD400-2 | REV. A

SCALE | SHEET 3 OF 4



1/2 U285
4013
CLOCK 4
U234-5
CDØ
4001
1/4 U281
+5V
4013
END
TR4
U217-5
1/2 U271
RES
U264
4040
C282
C283
+5V_D
U263
2764
CYMBAL 1
U262
2764
CYMBAL 2
C284
U261
2764
CYMBAL 3
U260
CYMB 4
NC
1/6 U270
4049
RT4
U219-2
SEL1
SEL2
SEL3
SEL4
8.2K X9
RIDE/CRASH
CHANNEL 4
U272
U273
U217-10
TR5
HIGH HAT
CHANNEL 5
VOL 5
U229-7
4049
1/4 U281
1/6 U270
RT5
U219-12
4001
4013
R2136
2.4K
1/2 U269
CDØ-CDI2
VOL 6
R2148
1ØK
U229-1
CLOCK 6
U235-5
C2100
C2101
U280
4040
U279
2764
CLAPS
TAMB.
U278
2764
COWBELL
CABASA
PERCUSSION
CHANNEL 6
1/2 U271
4013
TR6
U217-7
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RT6B
U219-10
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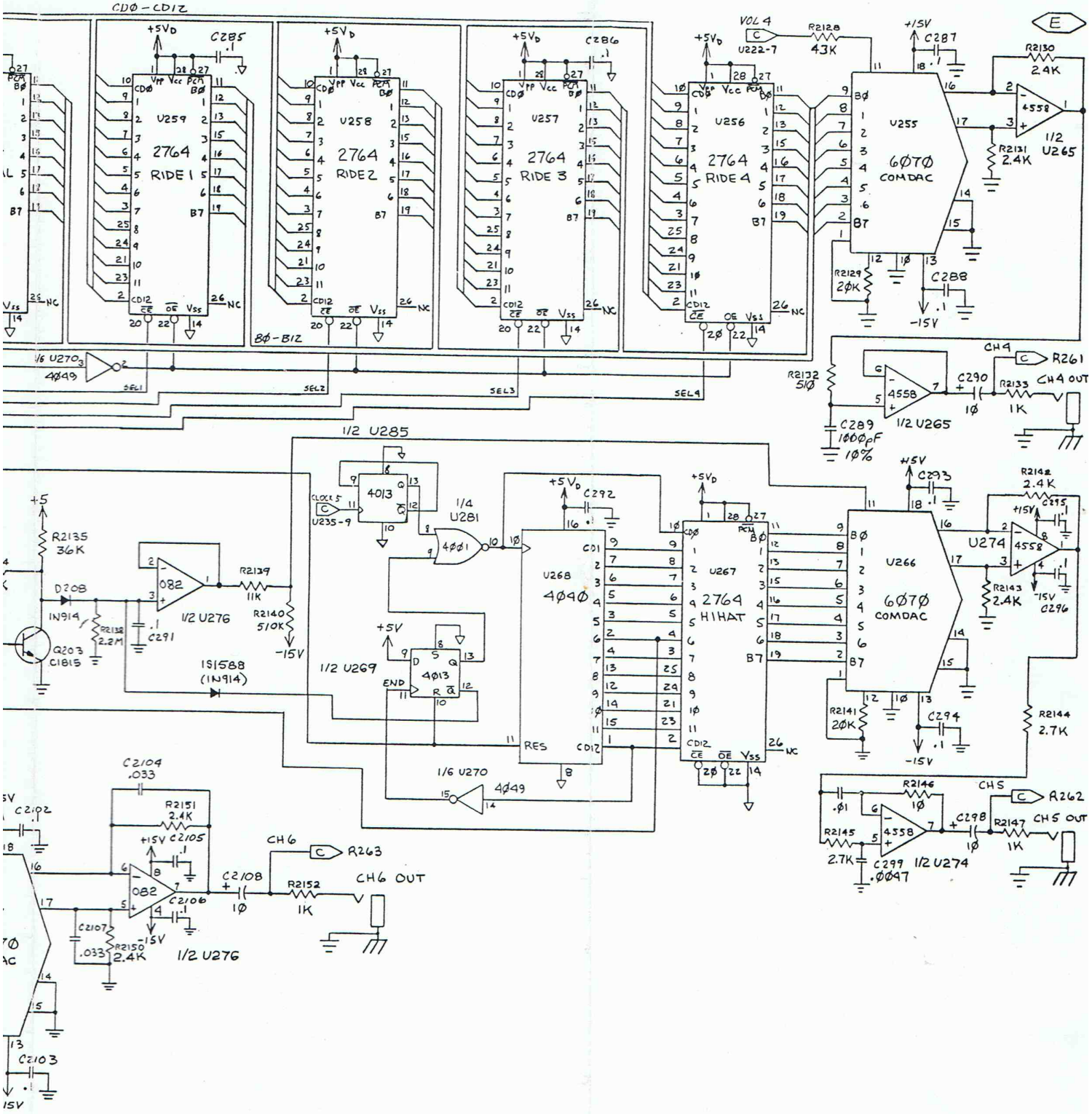
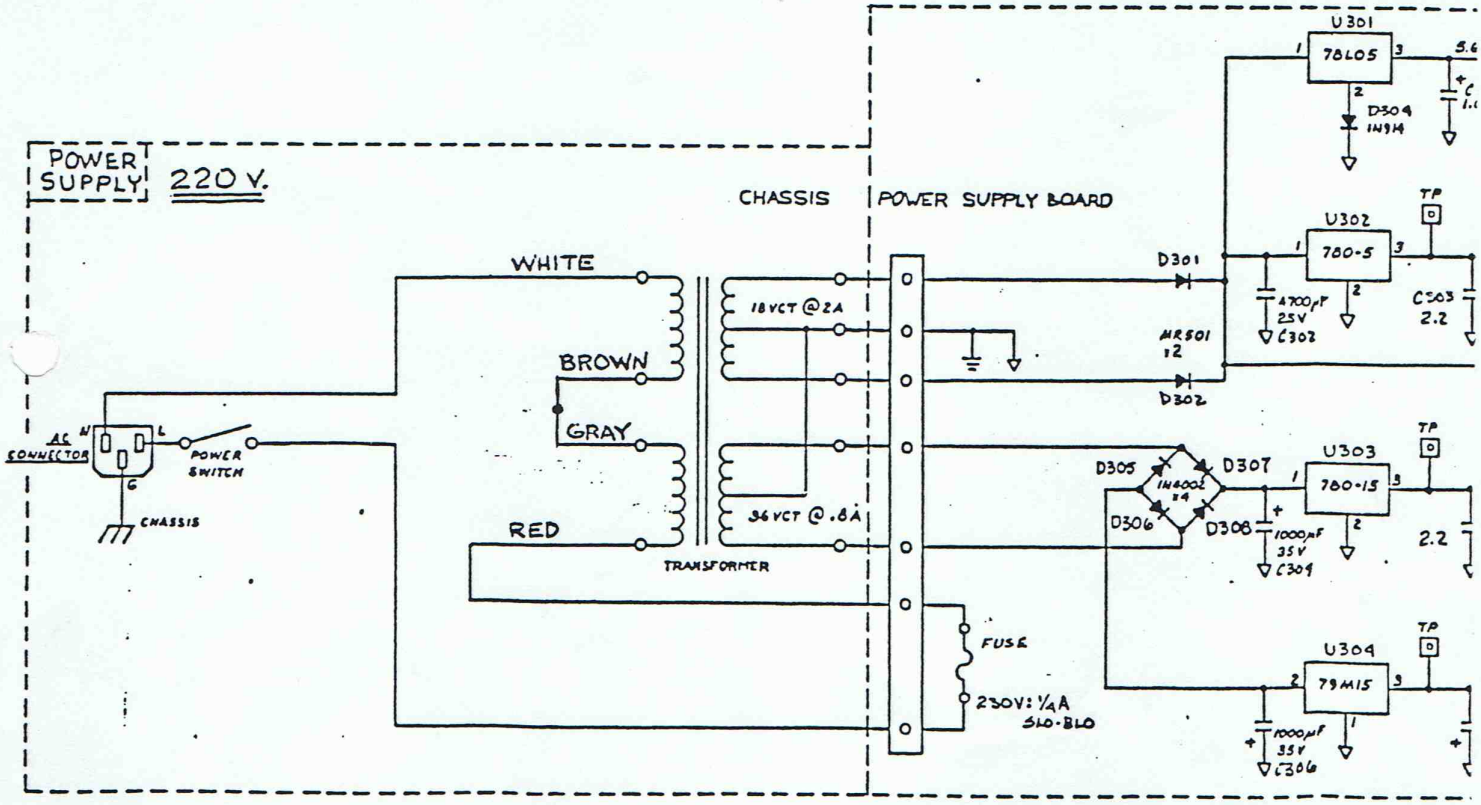
U219-5
BØ-B12
R2149
20K
8.2K X9

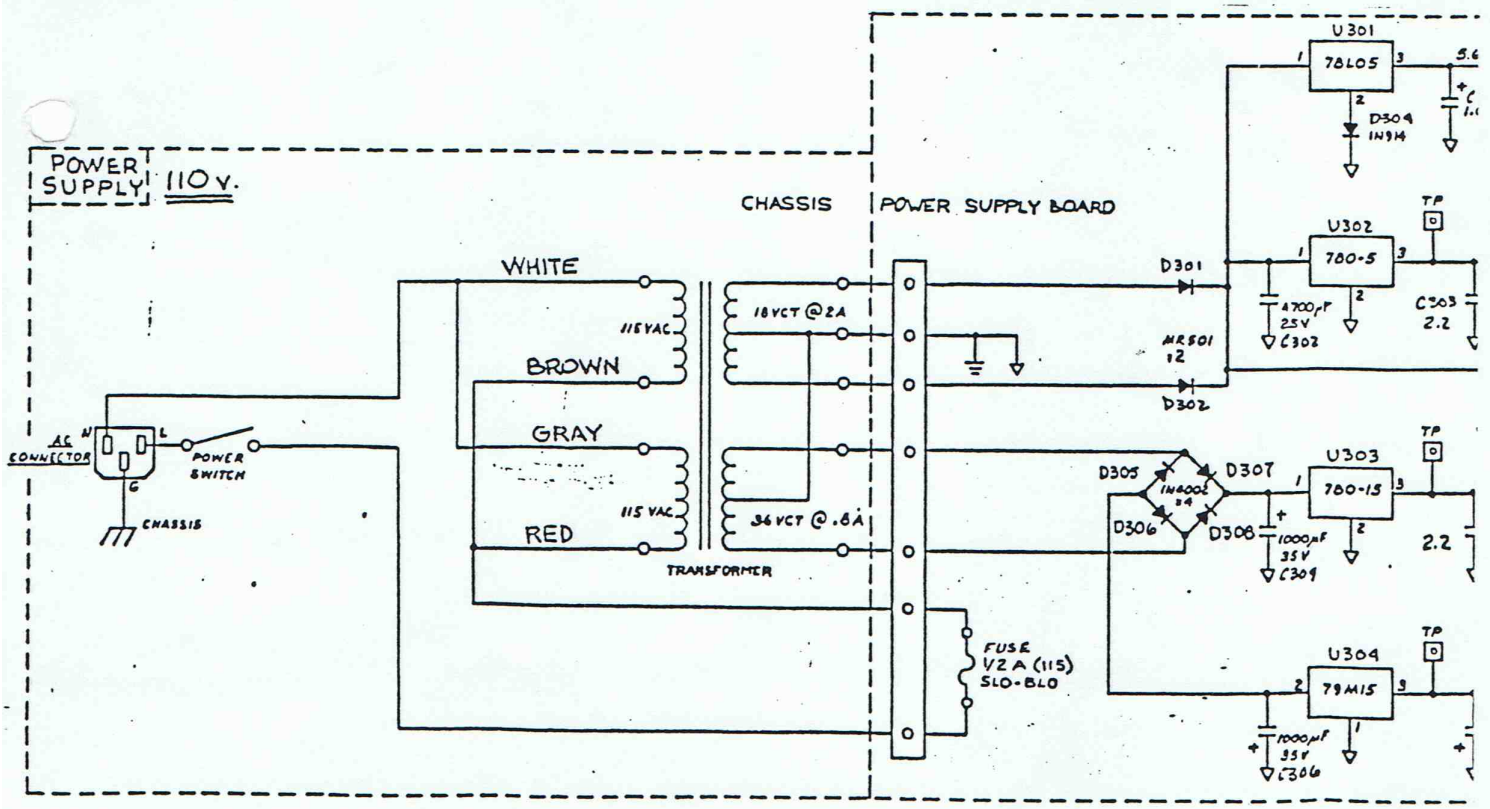


SEQUENTIAL CIRCUITS INC			
APPROVALS	DATE	TITLE	VOICES 4-6
DWN A	7/26/83	SIZE D	MODEL No 400
CHK SL/RD	11/28/83	DOCUMENT No	REV
DSN		SD400-2	A
PEN		SCALE	SHEET 4 OF 4
ISS			
12-23-83 A RELEASED 6-1-84			
DATE ECR No REVISION			

DRUMTRAKS MODEL 400

TRANSFORMER WIRING FOR 110 V. OR 220 V.





SEQUENTIAL CIRCUITS, Inc.
Publications Department

TN400-1
January, 1985

HOW TO UPDATE THE DRUMTRAKS' SOFTWARE

New software releases occur to either refine or enhance features, or to correct minor problems which have been revealed through extensive use. The specific features of each release are explained in the Drumtraks MIDIGUIDE (MG400).

Drumtraks software is updated by replacing one EPROM (Erasable Programmable Read-Only Memory). Depending on the new software version, the update may, or may not be covered under warranty. For details, read the Drumtraks MIDIGUIDE.

Handling EPROMs

It is not difficult to replace an EPROM. They are easy to find inside the chassis. Just work slowly and carefully. The EPROMs are shipped imbedded in conductive foam to neutralize static charges. To discharge yourself, touch the Drumtraks' metal chassis. You do not need to be too paranoid about handling the EPROMs. Try not to touch the pins.

Note: The "polarity" of the EPROM is marked by a notch on one end (which is sometimes covered by the label). When replacing, be sure to orient the EPROM correctly.

Preparation

CAUTION! SWITCH POWER OFF. For best protection, disconnect the power cable.

1. Remove the two front panel screws.

2. Lift the top panel back on its hinge.
   This exposes the Drumtraks' computer board (mounted on the bottom panel).

3. Identify the EPROM to be replaced (see figure below).

EPROM LOCATION

4. Note the orientation of the EPROM.
   The notch on one end of each EPROM is at the top.

Replacing the EPROMs

Note: It is best to use an integrated circuit remover which reaches under the edges at each end. (If you do much of this work, they are worth getting.) But most people do nicely using a small screwdriver to slowly pry up each end.

1. Carefully remove the EPROM. (You may have to work around the capacitor located near the notched edge of the EPROM.)

Note: Try to keep the EPROM parallel to the PCB. Lift the chip straight up so that no pins are bent.

Note: You will be billed $35 for each damaged EPROM.

CAUTION: When using a screwdriver, don't gouge the traces (on the PCB) which run under the socket.

2. Check that all the pins on the old EPROM are intact, and place it in the foam.

3. Check that the socket is not damaged. Check that there is no debris in or between the individual holes of the socket.

4. Check that the pins of the new EPROM are straight. The pins of new EPROMs tend to bend outward and must often be reshaped for accurate mating to the socket.

5. Orient the new EPROM correctly.

6. Place the new EPROM into the socket, but before pressing down, make sure that each pin is correctly centered in its hole. (Sometimes, pins can be trapped on the inside of the socket, too.)

7. Press down, again keeping the EPROM parallel to the board.

Testing

1. Lower the top panel, but don't replace the screws yet.

2. Switch power on and play a few drum patterns to confirm that the Drumtraks basically works.

3. Check the new features described in the accompanying MIDIGUIDE.

4. Perform a full functional test of the instrument. No patterns should have been affected.

5. If the Drumtraks tests OK, fasten the top panel.

Returning Old EPROMs

Note: Firmware updates are usually sold on a replacement basis. An RMA form is enclosed which must be returned with your EPROM, for proper credit.

1. On the form, check off the number of EPROMs you are returning.

2. Keep the gold copy.

3. Enclose the pink copy with the EPROM.

4. Carefully package the EPROM.

5. Mark the package on two sides with the RMA # (number).

Note: You will be billed $35 for each unreturned (or damaged) EPROM.