

JP-8 SERVICE NOTES

Second Edition
December, 1982

This Notes makes First Edition obsolete and consists of two parts:

Part 1 Previous First Edition pp.1—31

Part 2 Mainly applicable to JP-8 units with Serial Numbers

171700 and above pp.32—46

Parts List Change p.47

Appendix pp.48—50

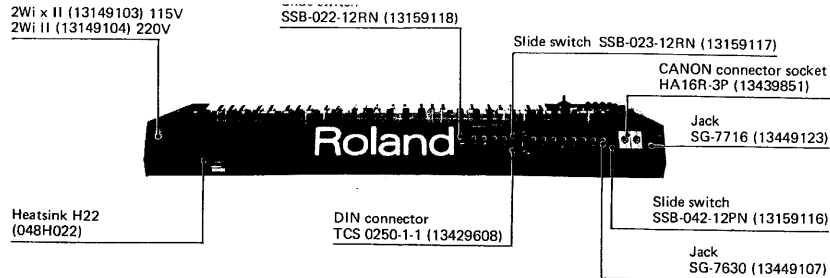
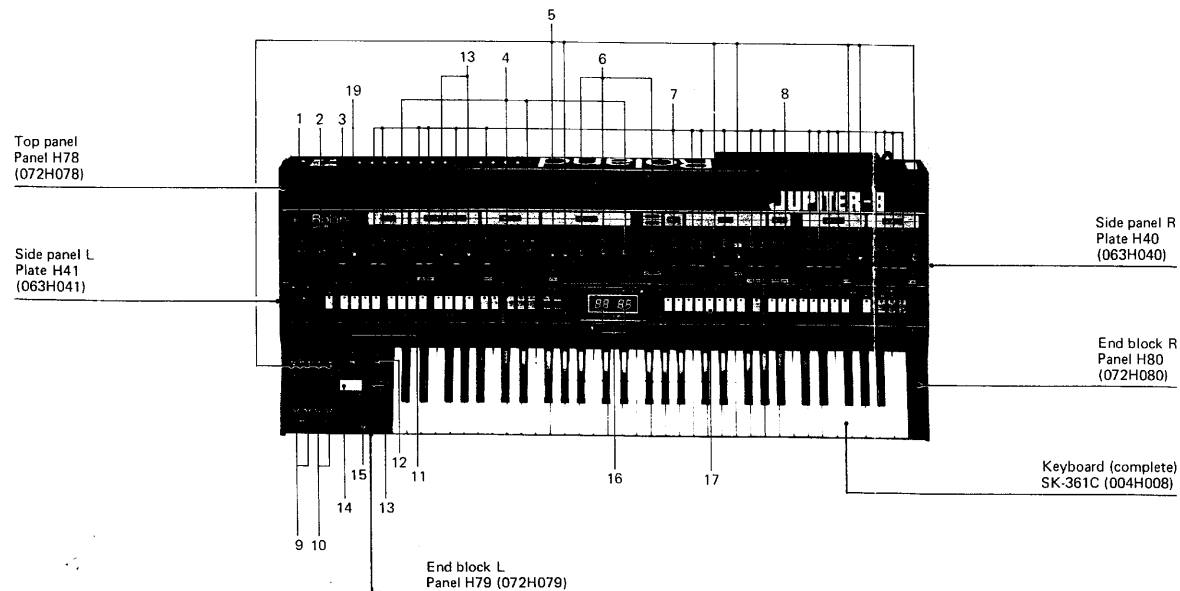
BEFORE READING

PLEASE CHECK FOR CHANGE INFORMATION
AND CONTENTS AT PAGES 32 AND 33
OF THIS NOTES.

SPECIFICATIONS

Keyboard: 61 Note, 5 Octaves
VCO
VCO-2 Fine Tune Range: ± 50 Cents
VCF
Slope: 12/Octave, 24/Octave
Key Follow: 0 - 120%
ENV
ENV-1, 2
Attack Time: 1ms - 5s
Decay Time: 1ms - 10s
Sustain Level: 0 - 100%
Release Time: 1ms - 10s
LFO
Rate: 0.05 - 40Hz
Delay Time: 0 - 4s
Master Tunable Range: $\pm 50\%$

Arpeggio Rate: 1 - 20Hz
Audio Outputs
Upper: 0dBm, 600 Ohm, Balanced
0dBm/-20dBm, 1k Ohm, Unbalanced
Lower: 0dBm, 600 Ohm, Balanced
0dBm/-20dBm, 1k Ohm, Unbalanced
Highest Note Output
CV: 0 - 5V
Gate: Off - 0V, On - +15V
Dimensions: 1063(W) x 485(D) x 120(H)mm
Weight: 22kg
Power Consumption: 90W

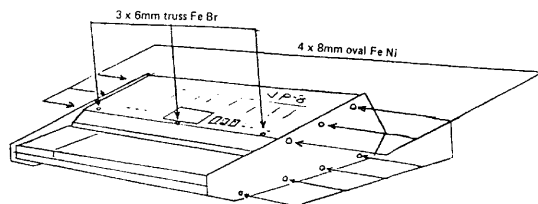


JP-8 PANEL PARTS LIST

1	Pot.	GM70R-K20B54 (50KB x 2) (13219812)
2	Pot.	GM70R-K20AC54 (50KA, C) (13219811)
3	Pot.	LFE9R-C16A55 (500KA) (13339414)
4	Switch	SRM1034-K15 (13119301)
5	Switch	SLE622-18PS (13139137)
6	Pot.	VM10R-K20B14 (10KB) (13219225)
7	Pot.	LFE9R-C16B14 (10KB) (13339415)
8	Switch	SOPR-24-12P (13159503)
9	Pot.	LFE9R-C16B54 (50KB) (13339413)
10	Pot.	MFE9R-C16B54 (50KB x 2) (13359302)
11	Pot.	VM10R-K20A55 (500KA) (13219231)
12	Pot.	VM10R-K20C54 (50KC) (13219243)
13	Switch	SLE623-18P (13139135)
14	Switch w/key top	KEH10003 (13129717) See Parts List for Key top and Switch
15	Bender assy	PB-4 (029-022)
16	Cover LED	H80 (065H080) LN526RA (15029404)
17	Switch	KHC11901 (13169601)
	Buttons	
	No.1, 38	RED (016H018)
	No.2-5, No.34-37	ORANGE (016H012)
	No.6-9, No.30-33	YELLOW (016H017)
	No.10-13, No.21-28	WHITE (016H010)
	No.14, 15, 29	GREEN (016H014)
	No.16-18, No.39-41	BLUE (016H013)
	No.19, 20	DARK BLUE (016H011)
18	Pot.	VM10A-K15B54 (50KB CT) (13229131)
19	Switch	SLE-622-18P (13139136)
	All rotary knobs	No.68 (016-078)
	All slider knobs	H4 (016H004)

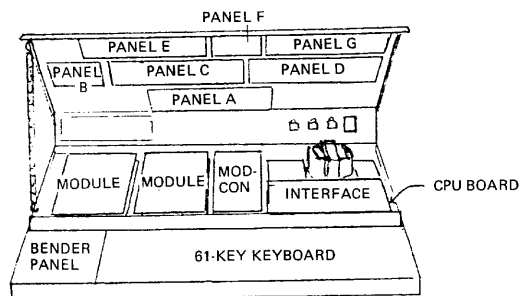
DISASSEMBLY

Remove screws ①, ② and ③.



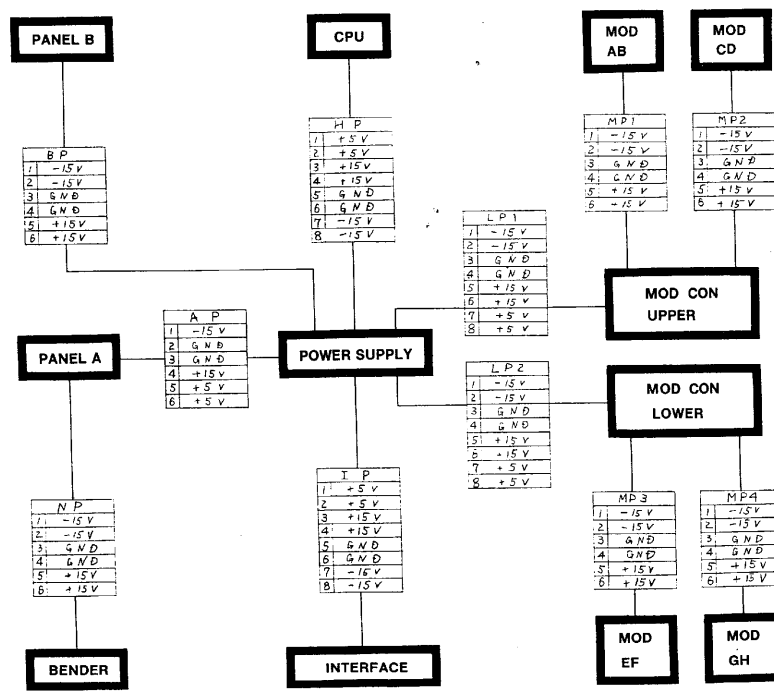
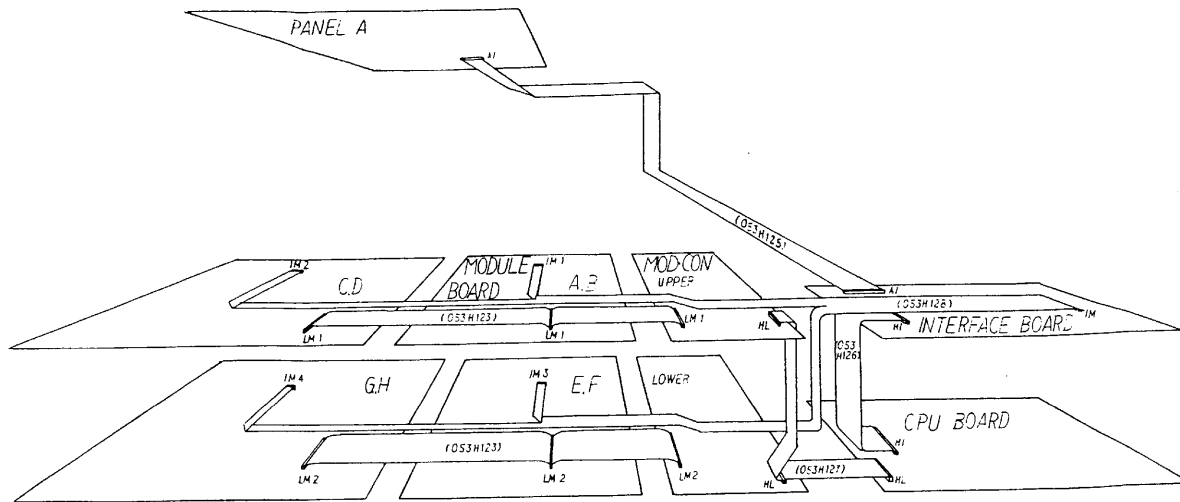
NOTE:

Preparation of a stay and a prop is recommended for a stable top panel rest.



PRECAUTIONS

- Do not pinch flat cables in the pcbs when closing panel assemblies. Prongs on PCBs will pierce humped cable, causing circuits to malfunction. Stretch rolling cable out.
- Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, PCBs are temperature-sensitive.



MOD A B
MOD C D

1	B M 1
2	OUT B
3	GND
4	OUT A

1	B M 1 2
2	OUT A
3	GND
4	OUT B
5	GND
6	OUT C
7	GND
8	OUT D

1	B M 2
2	OUT D
3	GND
4	OUT C

1	B M 2
2	OUT D
3	GND
4	OUT C

EXT JACK

1	B J 1
2	GND
3	BAL OUT LT.
4	" " L-
5	GND
6	BAL OUT UT
7	" " U-
8	GND
9	PHONES

1	B J 2
2	GND
3	U OUT
4	GND
5	L OUT
6	GND
7	MIX OUT

MODE F
MOD G H

1	B M 3
2	OUT F
3	GND
4	OUT E
5	GND

1	B M 3 4
2	OUT E
3	GND
4	OUT F
5	GND
6	OUT G
7	GND
8	OUT H

1	B M 4
2	OUT H
3	GND
4	OUT G
5	GND

1	B M 4
2	OUT H
3	GND
4	OUT G
5	GND

MOD CON
U L

1	A L 1
2	TUNE
3	VCO1 BEND
4	VCO2 BEND
5	VCO B LFO
6	VCF PEDAL
7	VCF MOD
8	EXP PEDAL
9	LFO U SEND
10	LFO L
11	GND

1	A L 2
2	TUNE
3	VCO1 BEND
4	VCO2 BEND
5	VCO B LFO
6	VCF PEDAL
7	VCF MOD
8	EXP PEDAL
9	LFO L SEND
10	LFO U
11	GND

BENDER

1	A N
2	COMPUTUNE
3	VCO1 BEND
4	VCO2 BEND
5	VCO B LFO U
6	" " L
7	" " L
8	LFO U
9	LFO L
10	GND
11	PORTA VR
12	PORTA U
13	PORTA L
14	GND

TUNE CONT

1	A T
2	TUNE VR ①
3	" " ②
4	" " ③
5	GND

EXT JACK

1	A J 1
2	GND
3	DIN SW RET
4	ARP CLK DIN
5	" " EXT
6	VCF PEDAL
7	EXP PEDAL
8	PORTA SW
9	HOLD

1	A J 2
2	GND
3	MEM.PROTECT
4	LOAD
5	DUMP
6	EXT CV
7	EXT GATE
8	DIN CLK IN
9	DIN START/STOP

PANEL B

1	A C 1
2	VCO1 RANGE-1
3	" " -φ
4	" " PWM-φ
5	" " -1
6	" " MOD-φ
7	" " -1
8	LFO WAVE-φ
9	" " -1
10	N.C.

1	A D 1
2	ENV2 K.FOLLOW
3	POLARITY
4	ENV1 K.FOLLOW
5	VCA LFO MOD-1
6	" " -φ
7	ENV 1/2
8	SLOPE
9	N.C.

1	A C 2
2	SOURCE MIX
3	VCO2 FINE
4	" " RANGE
5	VCO MOD CROSS
6	" " PWM
7	" " ENV
8	" " LFO
9	LFO DELAY T
10	RATE
11	VR.SUP
12	GND

1	A D 2
2	ENV 2 R
3	" " S
4	" " D
5	" " A
6	ENV 1 R
7	" " S
8	" " D
9	" " A

1	A C 3
2	VCO2 WAVE-1
3	" " -φ
4	VCO2 LF/NORM
5	SYNCHRO
6	VCO1 WAVE-1
7	" " -φ

1	A D 3
2	VCA LEVEL
3	" " LFO
4	" " ENV
5	" " RESO
6	" " CUTOFF
7	HPF
8	VR.SUP
9	GND
10	GND

1	A E 1
2	SW DATA -5
3	" " -4
4	" " -3
5	" " -2
6	" " -1
7	LED DATA -5
8	" " -4
9	" " -3
10	" " -2
11	" " -1
12	" " -φ

1	A E 2
2	MATRIX BUS-φ
3	" " -1
4	" " -2
5	" " -3
6	" " -4
7	N.C.

1	A F 1
2	NUM DATA -7
3	" " -6
4	" " -5
5	" " -4
6	" " -3
7	" " -2
8	" " -1
9	" " -φ

1	A F 2
2	NUM BUS -7
3	" " -φ
4	" " -3
5	" " -2
6	" " -1
7	N.C.

PANEL A

1	A G 1
2	+5V
3	FSK LED
4	SW DATA -5
5	" " -4
6	" " -3
7	" " -2
8	" " -1
9	" " -φ
10	LED DATA -5
11	" " -4
12	" " -3
13	" " -2
14	" " -1
15	" " -φ

1	A G 2
2	MATRIX BUS-4
3	" " -5
4	" " -6
5	" " -7

1	A I
2	FUNC SW
3	DIGITAL IN 2
4	DIGITAL IN 3
5	DOT LED
6	NUM LED
7	MATRIX
8	ANALOG SEL
9	GND
10	GND
11	VR DATA
12	VR DATA
13	GND
14	GND
15	φ 0
16	φ 1
17	φ 2
18	φ 3
19	φ 4
20	φ 5
21	φ 6
22	φ 7
23	GND
24	COMPUTUNE
25	PORTA VR
26	PORTA F.SW
27	PORTA U
28	PORTA L
29	SPLIT
30	HOLD
31	ARP CONT.
32	ARP CLK
33	EXT GATE
34	GND
35	EXT CV
36	GND
37	DUMP
38	LOAD
39	FSK LED
40	MEM.PROTECT

PANEL C

PANEL D

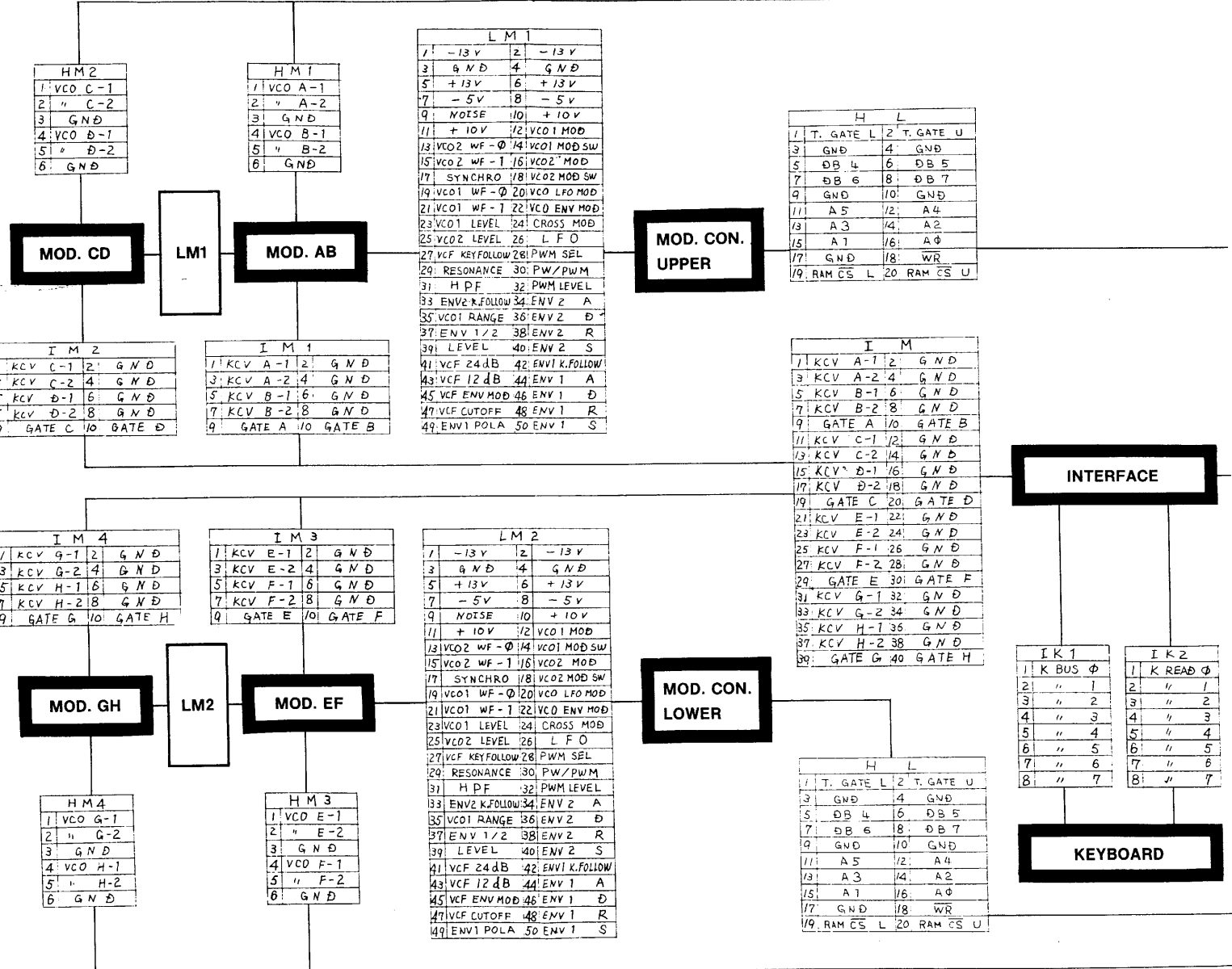
PANEL E

PANEL F

PANEL G

INTERFACE

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z



HM2	
1	VCO C-1
2	" C-2
3	GND
4	VCO D-1
5	" D-2
6	GND

HM1	
1	VCO A-1
2	" A-2
3	GND
4	VCO B-1
5	" B-2
6	GND

LM1	
1	-13V
2	-13V
3	GND
4	GND
5	+13V
6	+13V
7	-5V
8	-5V
9	NOISE
10	+10V
11	+10V
12	VCO1 MOD
13	VCO2 WF-Φ
14	VCO1 MOD SW
15	VCO2 WF-1
16	VCO2 MOD
17	SYNCHRO
18	VCO2 MOD SW
19	VCO1 WF-Φ
20	VCO LFO MOD
21	VCO1 WF-1
22	VCO ENV MOD
23	VCO1 LEVEL
24	CROSS MOD
25	VCO2 LEVEL
26	LFO
27	VCF KEY FOLLOW
28	PWM SEL
29	RESONANCE
30	PW/PWM
31	H PF
32	PWM LEVEL
33	ENV2 R.FOLLOW
34	ENV 2 A
35	VCO1 RANGE
36	ENV 2 D
37	ENV 1/2
38	ENV 2 R
39	LEVEL
40	ENV 2 S
41	VCF 24dB
42	ENV1 K.FOLLOW
43	VCF 12dB
44	ENV 1 A
45	VCF ENV MOD
46	ENV 1 D
47	VCF CUTOFF
48	ENV 1 R
49	ENV1 POLA
50	ENV 1 S

H L	
1	T. GATE L
2	T. GATE U
3	GND
4	GND
5	DB 4
6	DB 5
7	DB 6
8	DB 7
9	GND
10	GND
11	A5
12	A4
13	A3
14	A2
15	A1
16	A0
17	GND
18	WR
19	RAM CS L
20	RAM CS U

IM2	
1	KCV C-1
2	GND
3	KCV C-2
4	GND
5	KCV D-1
6	GND
7	KCV D-2
8	GND
9	GATE C
10	GATE D

IM1	
1	KCV A-1
2	GND
3	KCV A-2
4	GND
5	KCV B-1
6	GND
7	KCV B-2
8	GND
9	GATE A
10	GATE B

IM	
1	KCV A-1
2	GND
3	KCV A-2
4	GND
5	KCV B-1
6	GND
7	KCV B-2
8	GND
9	GATE A
10	GATE B
11	KCV C-1
12	GND
13	KCV C-2
14	GND
15	KCV D-1
16	GND
17	KCV D-2
18	GND
19	GATE C
20	GATE D
21	KCV E-1
22	GND
23	KCV E-2
24	GND
25	KCV F-1
26	GND
27	KCV F-2
28	GND
29	GATE E
30	GATE F
31	KCV G-1
32	GND
33	KCV G-2
34	GND
35	KCV H-1
36	GND
37	KCV H-2
38	GND
39	GATE G
40	GATE H

IM4	
1	KCV G-1
2	GND
3	KCV G-2
4	GND
5	KCV H-1
6	GND
7	KCV H-2
8	GND
9	GATE G
10	GATE H

IM3	
1	KCV E-1
2	GND
3	KCV E-2
4	GND
5	KCV F-1
6	GND
7	KCV F-2
8	GND
9	GATE E
10	GATE F

LM2	
1	-13V
2	-13V
3	GND
4	GND
5	+13V
6	+13V
7	-5V
8	-5V
9	NOISE
10	+10V
11	+10V
12	VCO1 MOD
13	VCO2 WF-Φ
14	VCO1 MOD SW
15	VCO2 WF-1
16	VCO2 MOD
17	SYNCHRO
18	VCO2 MOD SW
19	VCO1 WF-Φ
20	VCO LFO MOD
21	VCO1 WF-1
22	VCO ENV MOD
23	VCO1 LEVEL
24	CROSS MOD
25	VCO2 LEVEL
26	LFO
27	VCF KEY FOLLOW
28	PWM SEL
29	RESONANCE
30	PW/PWM
31	H PF
32	PWM LEVEL
33	ENV2 R.FOLLOW
34	ENV 2 A
35	VCO1 RANGE
36	ENV 2 D
37	ENV 1/2
38	ENV 2 R
39	LEVEL
40	ENV 2 S
41	VCF 24dB
42	ENV1 K.FOLLOW
43	VCF 12dB
44	ENV 1 A
45	VCF ENV MOD
46	ENV 1 D
47	VCF CUTOFF
48	ENV 1 R
49	ENV1 POLA
50	ENV 1 S

H L	
1	T. GATE L
2	T. GATE U
3	GND
4	GND
5	DB 4
6	DB 5
7	DB 6
8	DB 7
9	GND
10	GND
11	A5
12	A4
13	A3
14	A2
15	A1
16	A0
17	GND
18	WR
19	RAM CS L
20	RAM CS U

IK1	
1	K BUS Φ
2	" 1
3	" 2
4	" 3
5	" 4
6	" 5
7	" 6
8	" 7

IK2	
1	K READ Φ
2	" 1
3	" 2
4	" 3
5	" 4
6	" 5
7	" 6
8	" 7

1 2 3 4 5 6 7 8 9 10 11 12 13

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z

HM12	
1	VCO A-1
2	" A-2
3	GND
4	VCO B-1
5	" B-2
6	GND
7	VCO C-1
8	" C-2
9	GND
10	VCO D-1
11	" D-2
12	GND

H		I	
1	Φ	2	GND
3	R D	4	I/O REQ
5	WR	6	RF SH
7	MREQ	8	RESET
9	M I	10	NMI
11	BUSREQ	12	BUSAK
13	GND	14	GND
15	Δ 0	16	Δ 1
17	Δ 2	18	Δ 3
19	Δ 4	20	Δ 5
21	Δ 6	22	Δ 7
23	GND	24	GND
25	A 0	26	A 1
27	A 2	28	A 3
29	A 4	30	A 5
31	A 6	32	A 7
33	A 8	34	A 9
35	A 10	36	A 11
37	A 12	38	A 13
39	A 14	40	A 15
41	MEM. PROTECT	42	TAPE OUT
43	TAPE READ	44	FSK LED
45	N.C.	46	N.C.
47	T. GATE L	48	T. GATE U
49	+5 V	50	+5 V

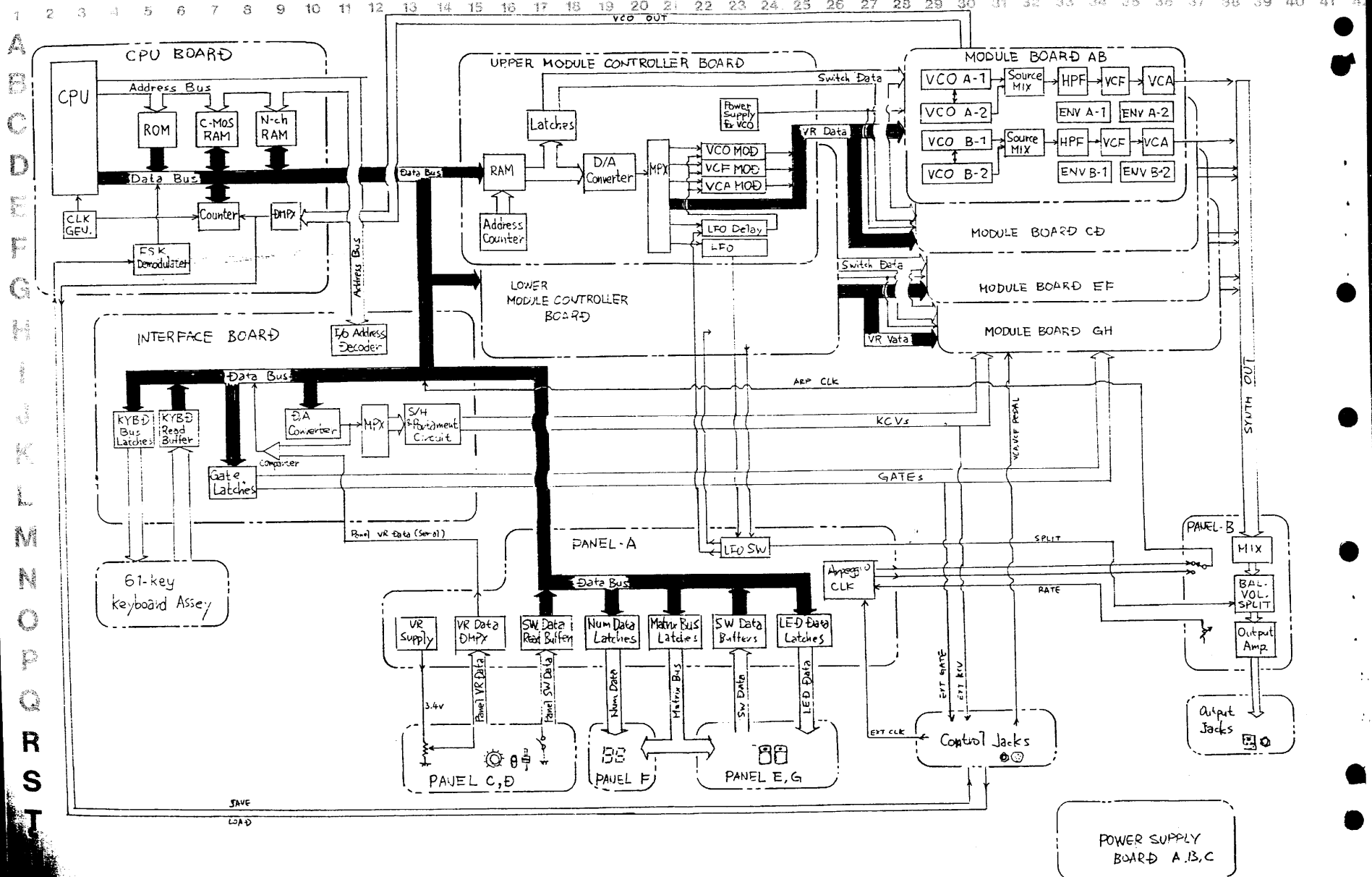
CPU BOARD

HM34	
1	VCO E-1
2	" E-2
3	GND
4	VCO F-1
5	" F-2
6	GND
7	VCO G-1
8	" G-2
9	GND
10	VCO H-1
11	" H-2
12	GND

WIRING DATA TABLE

CONNECTOR	PINS	P C B	
		from	to
AB	8	PANEL A	PANEL B
AC1	9	"	PANEL C
AC2	12	"	"
AC3	6	"	"
AD1	8	"	PANEL D
AD2	8	"	"
AD3	10	"	"
AE1	12	"	PANEL E
AE2	6	"	"
AF1	8	"	PANEL F
AF2	5	"	"
AG1	14	"	PANEL G
AG2	4	"	"
AI	40J	"	INTERFACE
AJ1	10	"	EXT JACK
AJ2	9	"	"
AL1	10	"	MOD CON U
AL2	10	"	MOD CON L
AN	14	"	BENDER
AP	6	"	POWER
BJ1	8	PANEL B	EXT JACK
BJ2	6	"	"
BM12	8 [4 BM2 [4	PANEL B	MODULE AB " CD
BM34	8 [4 BM3 [4 BM4 [4	PANEL B	" EF " GH
BP	6	PANEL B	PANEL A
HI	50J	C P U	INTERFACE
HL	20J	"	MOD CON
HM12	12 [6 HM1 [6 HM2 [6	C P U	MODULE AB " CD
HM34	12 [6 HM3 [6 HM4 [6	C P U	" EF " GH
HP	8	C P U	POWER
IK1	8	INTERFACE	KEYBOARD
IK2	8	"	"
IM	40J [10J IM1 [10J IM2 [10J IM3 [10J IM4 [10J	INTERFACE	MODULE AB " CD " EF " GH
IP	8	INTERFACE	POWER
LM1	50J	MOD CON U	MODULE ABCD
LM2	50J	" L	MODULE EFGH
LP1	8	" U	POWER
LP2	8	" L	"
MP1	6	MODULE AB	MOD CON U
MP2	6	" CD	"
MP3	6	" EF	MOD CON L
MP4	6	" GH	"
NP	6	BENDER	PANEL A
AT	4	PANEL A	TUNE VR

JP-8 FUNCTIONAL DIAGRAM

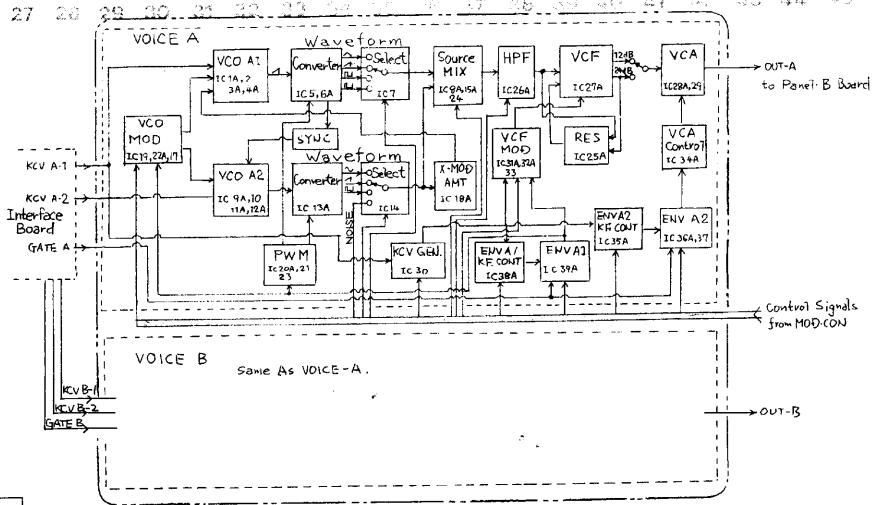


A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T

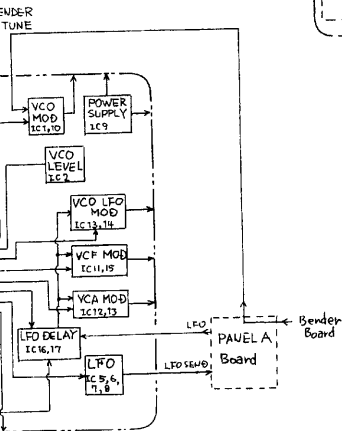
SAVE
LOAD

POWER SUPPLY BOARD A,B,C

22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48

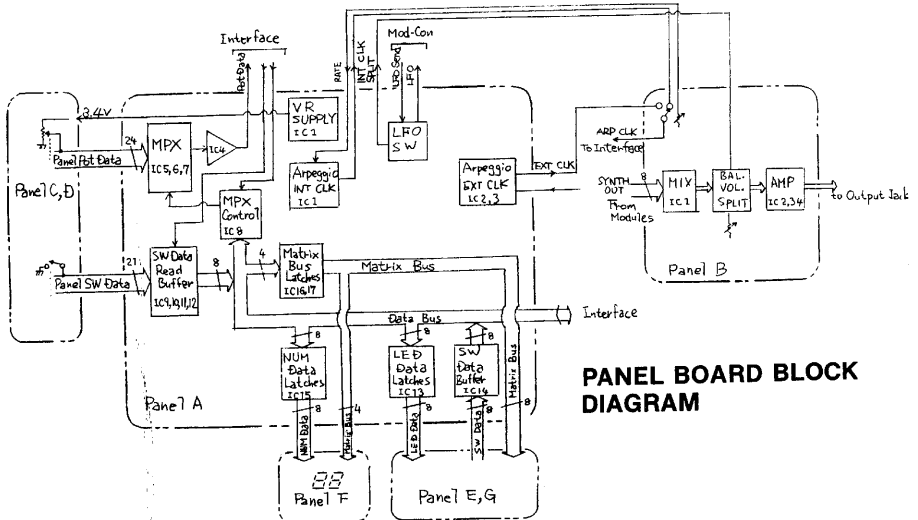


MODULE BOARD BLOCK DIAGRAM



BENDER BOARD BLOCK DIAGRAM

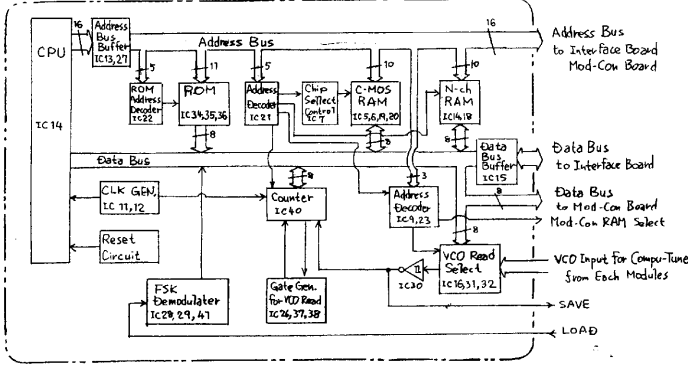
DESTINATION MODULE BOARD.



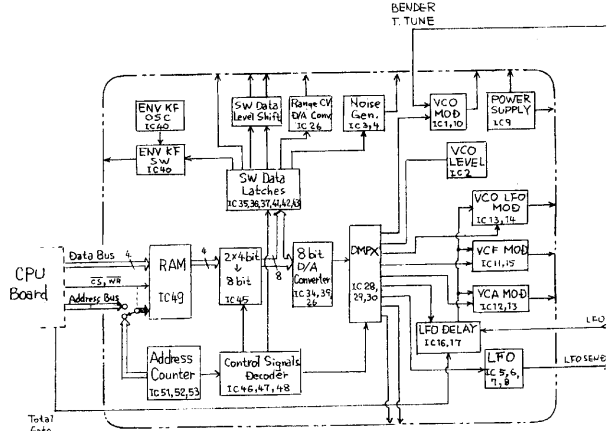
PANEL BOARD BLOCK DIAGRAM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

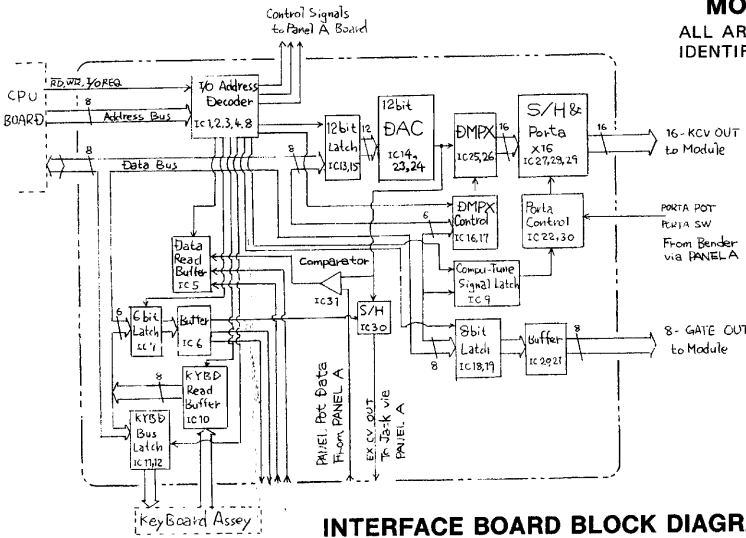
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z



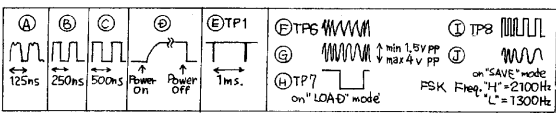
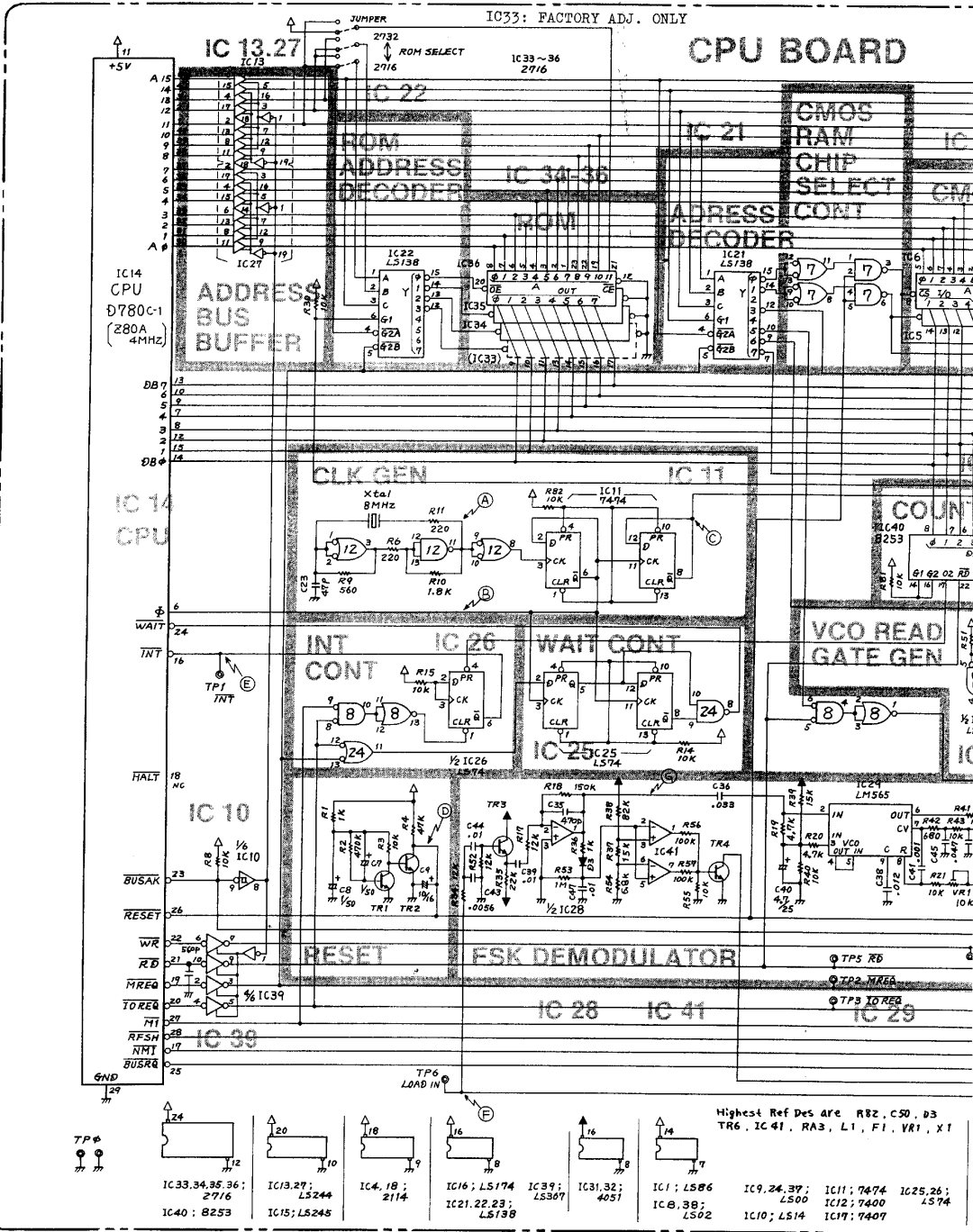
CPU BOARD BLOCK DIAGRAM

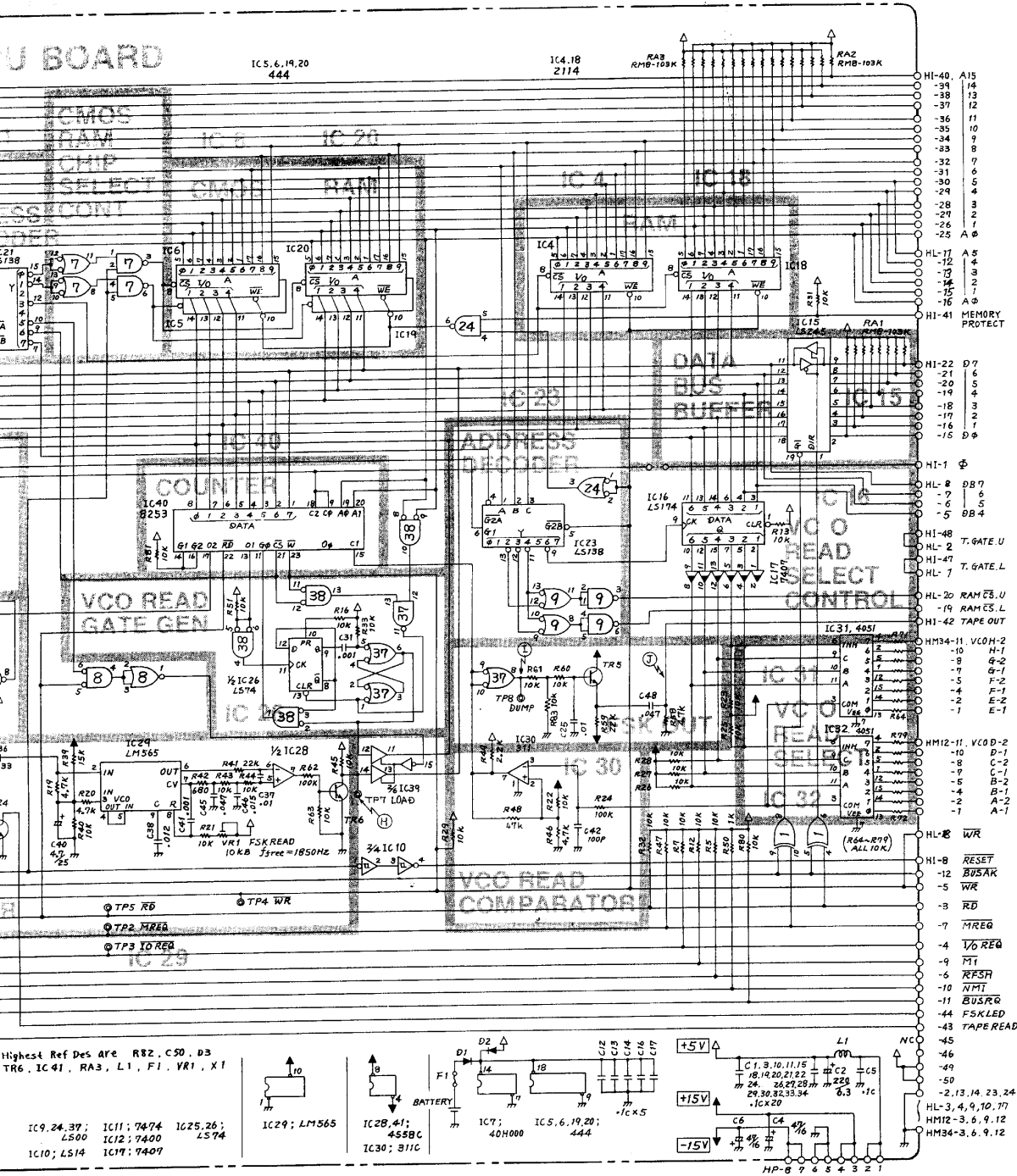


MOD-CON BOARD BLOCK DIAGRAM
ALL ARROWS HAVING NO DESTINATION IDENTIFIER CONNECT TO MODULE BOARD.



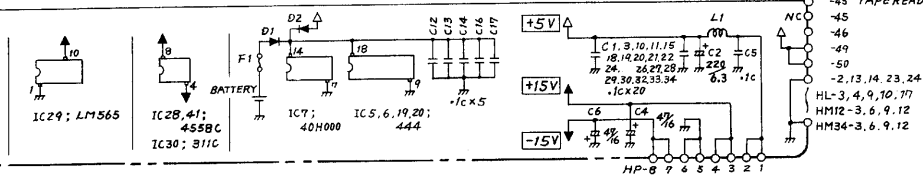
INTERFACE BOARD BLOCK DIAGRAM





Highest Ref Des are R82, C50, D3, TR6, IC41, RA3, L1, F1, VR1, X1

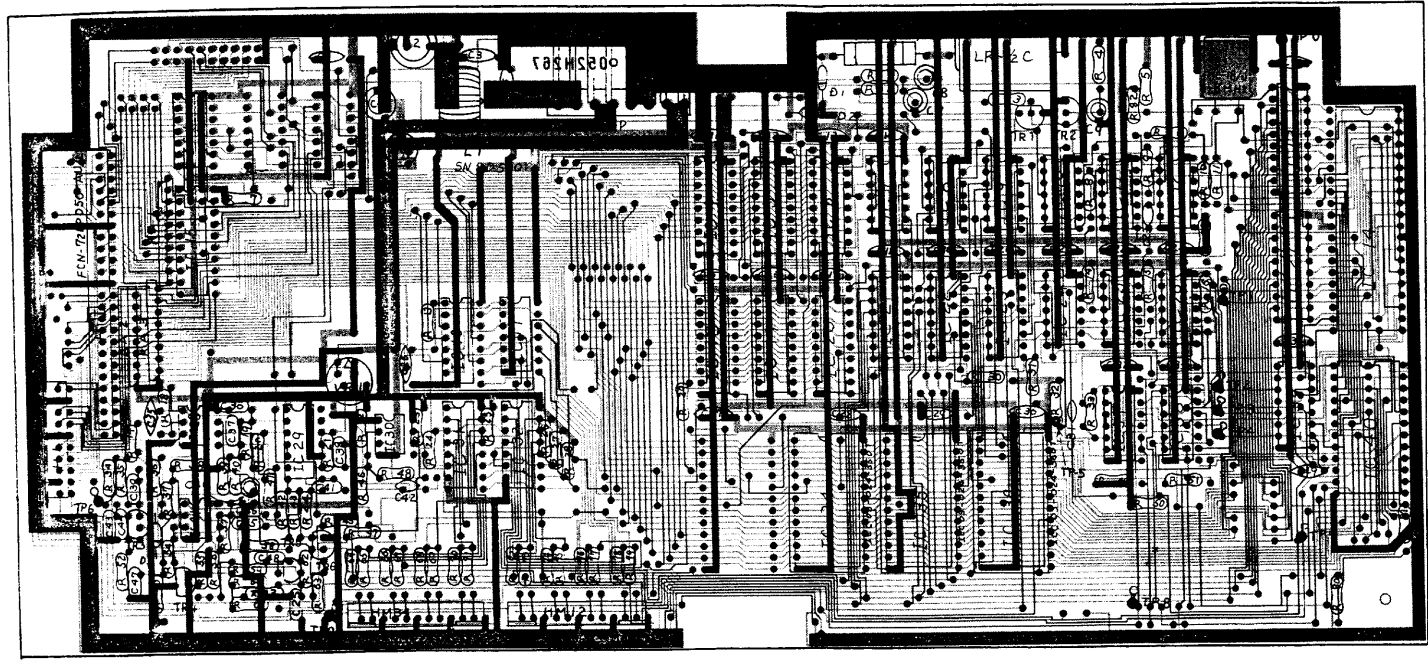
- IC9, 24, 37; L500
- IC11; 7474
- IC25, 26; L574
- IC10; LS14
- IC19; 7407
- IC29; LM565
- IC28, 41; 4558C
- IC30; 311C
- IC7; 40H000
- IC5, 6, 19, 20; 444
- ICx5






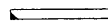


LSI 7400, 7401, 7402, 7403, 7404, 7405, 7406, 7407, 7408, 7409, 7410, 7411, 7412, 7413, 7414, 7415, 7416, 7417, 7418, 7419, 7420, 7421, 7422, 7423, 7424, 7425, 7426, 7427, 7428, 7429, 7430, 7431, 7432, 7433, 7434, 7435, 7436, 7437, 7438, 7439, 7440, 7441, 7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 7450, 7451, 7452, 7453, 7454, 7455, 7456, 7457, 7458, 7459, 7460, 7461, 7462, 7463, 7464, 7465, 7466, 7467, 7468, 7469, 7470, 7471, 7472, 7473, 7474, 7475, 7476, 7477, 7478, 7479, 7480, 7481, 7482, 7483, 7484, 7485, 7486, 7487, 7488, 7489, 7490, 7491, 7492, 7493, 7494, 7495, 7496, 7497, 7498, 7499, 7500.

CPU BOARD OPH121(149H121)(pcb 052H267)

A
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U
V
W
X
Y
Z



-  R25J
-  25C1815-GR
-  LC-2S
-  SR19R
-  .52473
-  RMB-103K

Refer to Page 38 for:
 CPU CHANGE INFORMATION
 CAUTIONS ON MODULE CONTROLLER BOARD REPLACEMENT
 RAM (MOD CON BOARD) REPLACEMENT
 CPU BOARD WILL BE AFFECTED BY THESE REPLACEMENTS

MODULE CONTROLLER

OPH123(149H123) (pcb 052H269)

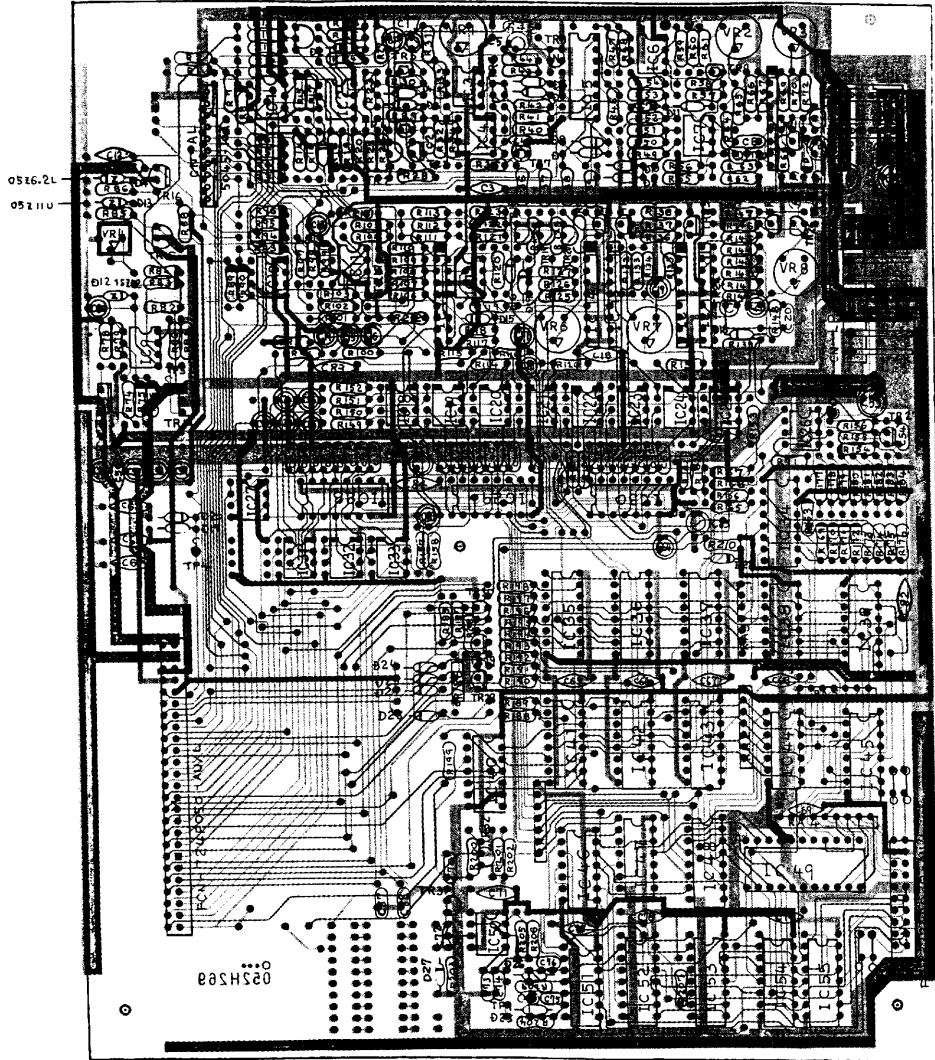
SN 090600-192099

REFER TO PAGES

49-50 for SN up to 090599

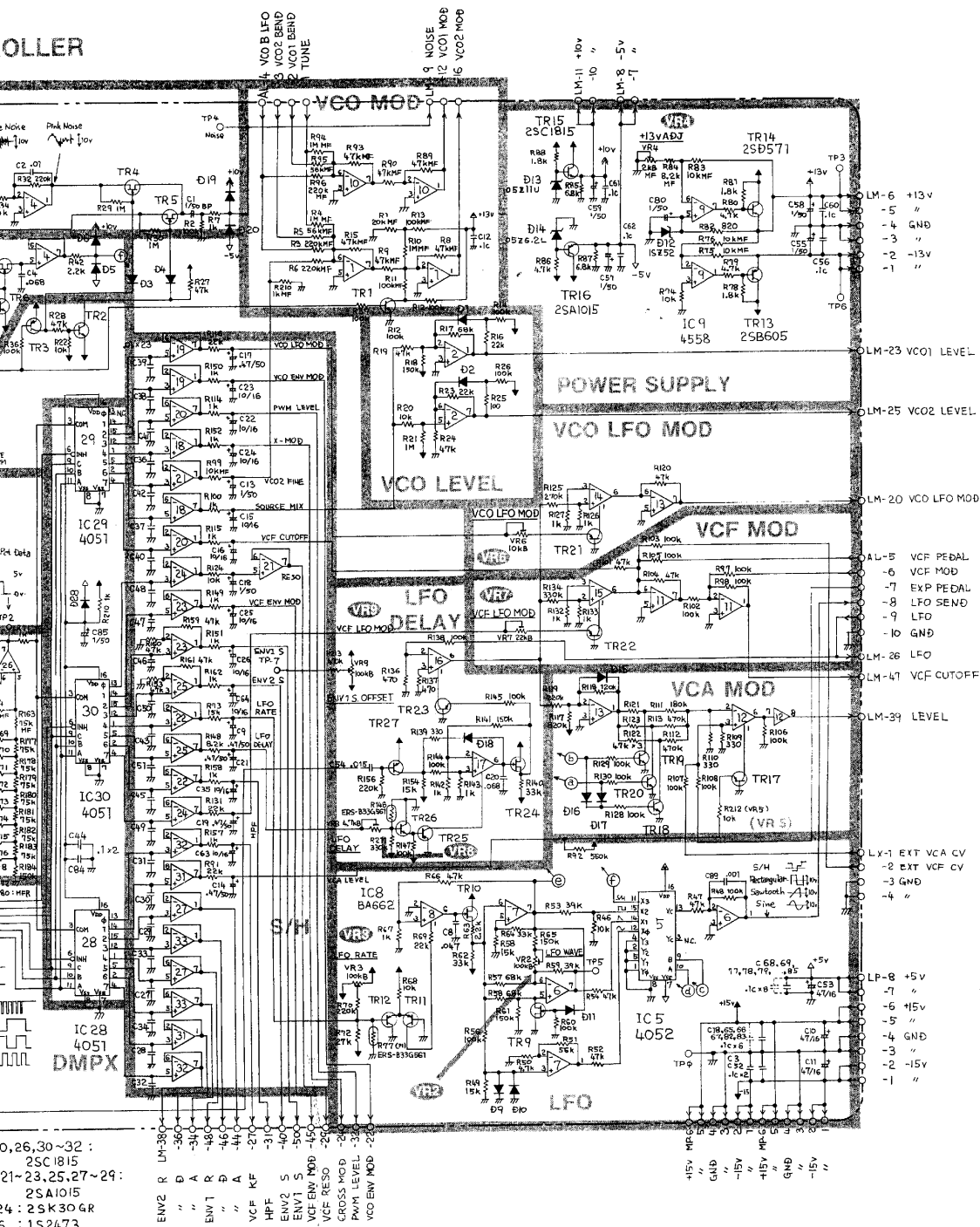
36-37 for SN 202100-up

37-38 for PCB or RAM REPLACEMENT



- selected on current leakage white dot
- R50J
- 1/4w carbon R25
- 1/4w metal film CRB25FX
- diosister ERS-C33 G561
- 1S2473
- zener diode
- 5R19A
- ET-6P
- 25A1015-GR
- 25C1815-GR
- 25C945 selected for Noise
- 25K30A-GR
- 25K117-GR
- 25B605
- 25D571
- BA662
- Resistor array
- BA662A selected on offset
- bi-polar
- test point LC-2-5

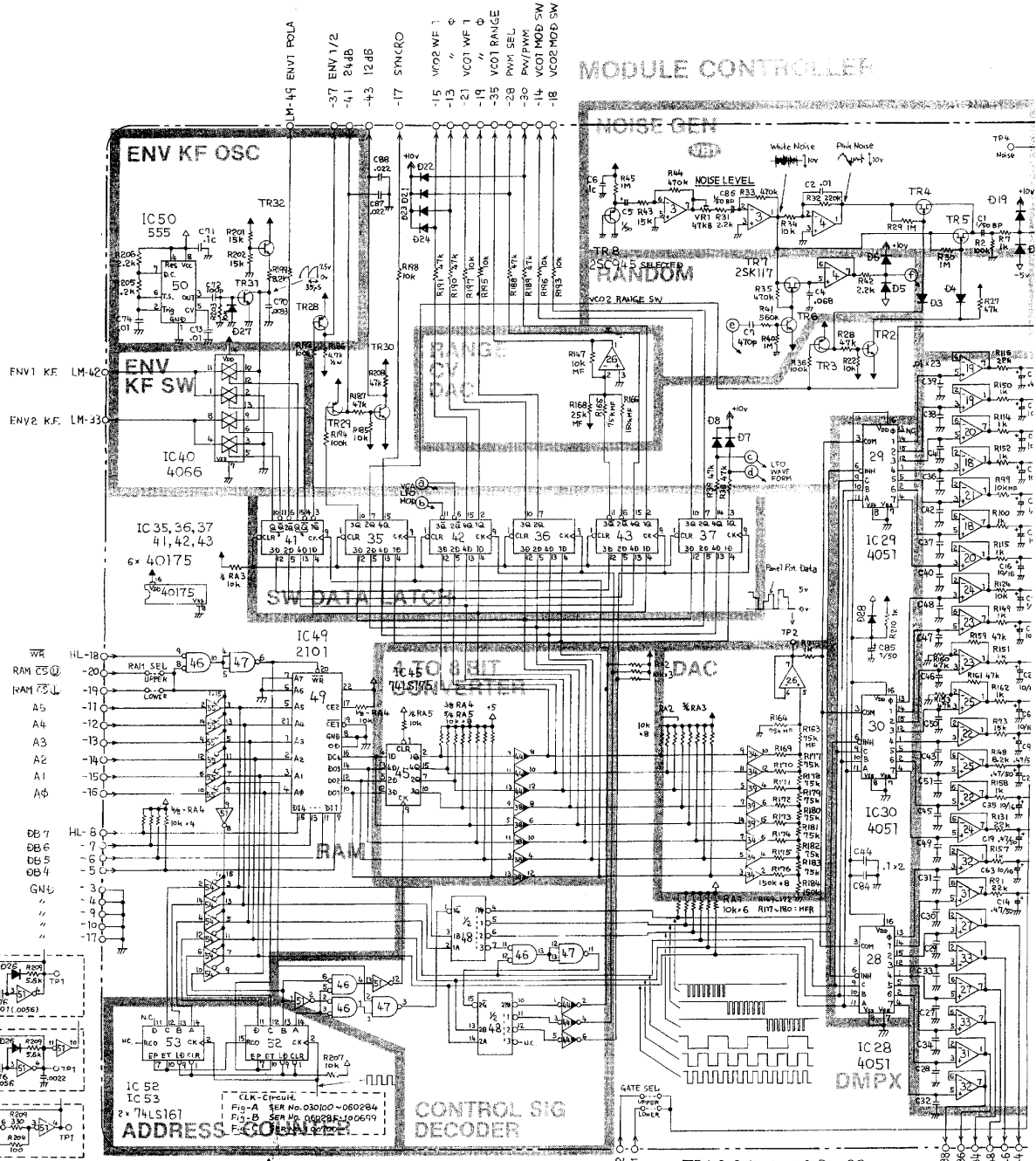
OLLER



- 0,26,30~32 : 2SC1815
- 21~23,25,27~29 : 2SA1015
- 24 : 2SK306R
- 5 : 1S2473

DES : IC55, TR32, D27, C88, R212, RA 5, VR 9

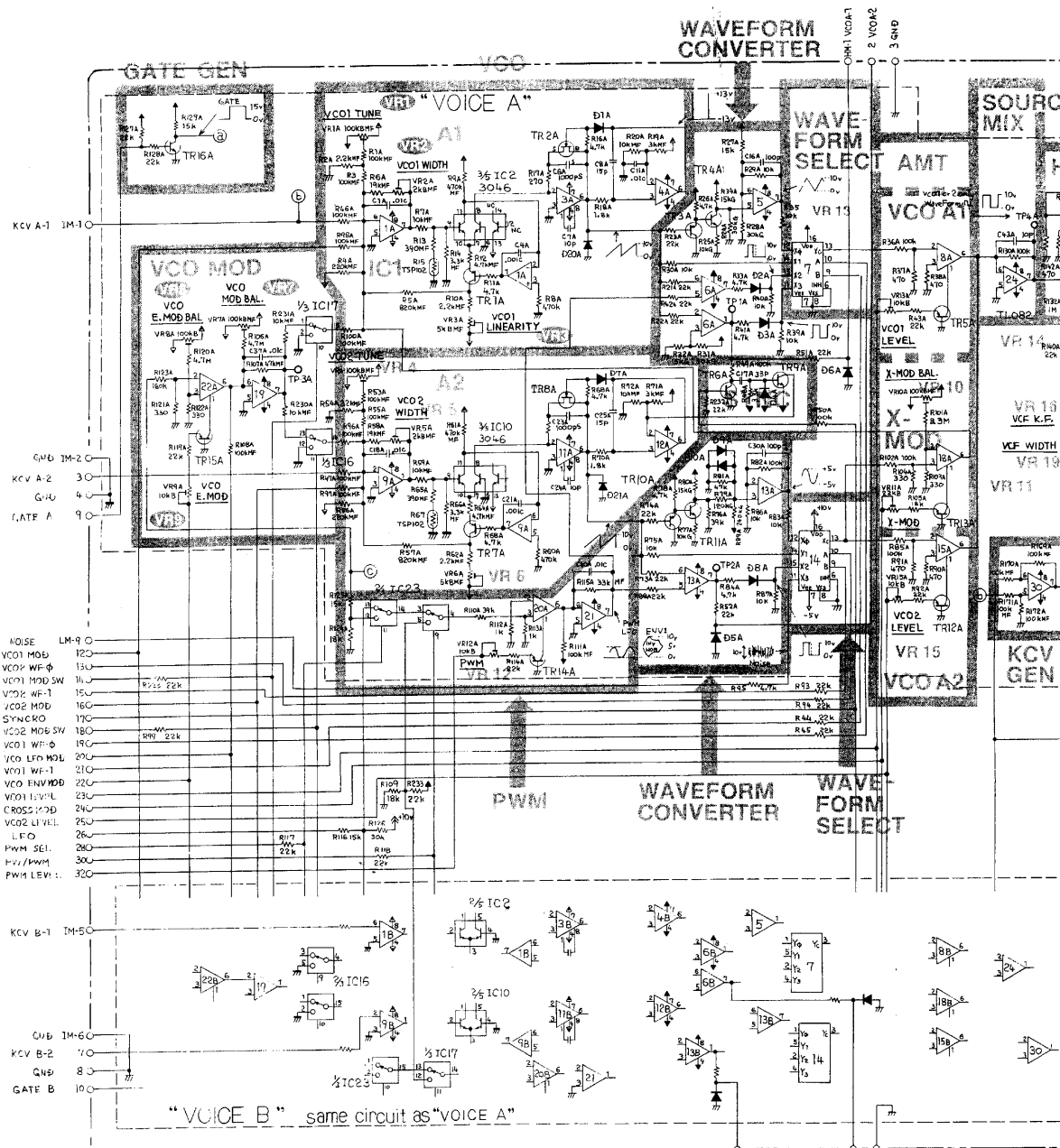
MODULE CONTROLLER



- IC 1, 2, 6, 9, 10, 11, 13 : 4558
- IC 3, 4, 7, 18 - 27, 31 - 33: TL082
- IC 8, 12, 14, 15 - 17 : BA662
- IC 34, 39 : 4050
- IC 38, 44 : 7407
- IC 46 : 74LS02
- IC 47 : 74LS00
- IC 51 : 74LS04
- IC 54, 55 : 74LS367

- IC 8, 7, 4, 15, 17 : BA662
- IC 12, 16 : BA662

- TR 1, 2, 6, 18 - 20, 26, 30 - 32 : 2SC1815
 - TR 3, 11, 12, 17, 21 - 23, 25, 27 - 29 : 2SA1015
 - TR 4, 5, 9, 10, 24 : 2SK304R
 - D1 - 11, 15 - 26 : 1S2473
- HIGHEST REF DES : IC55, TR32, D27, C88, R212

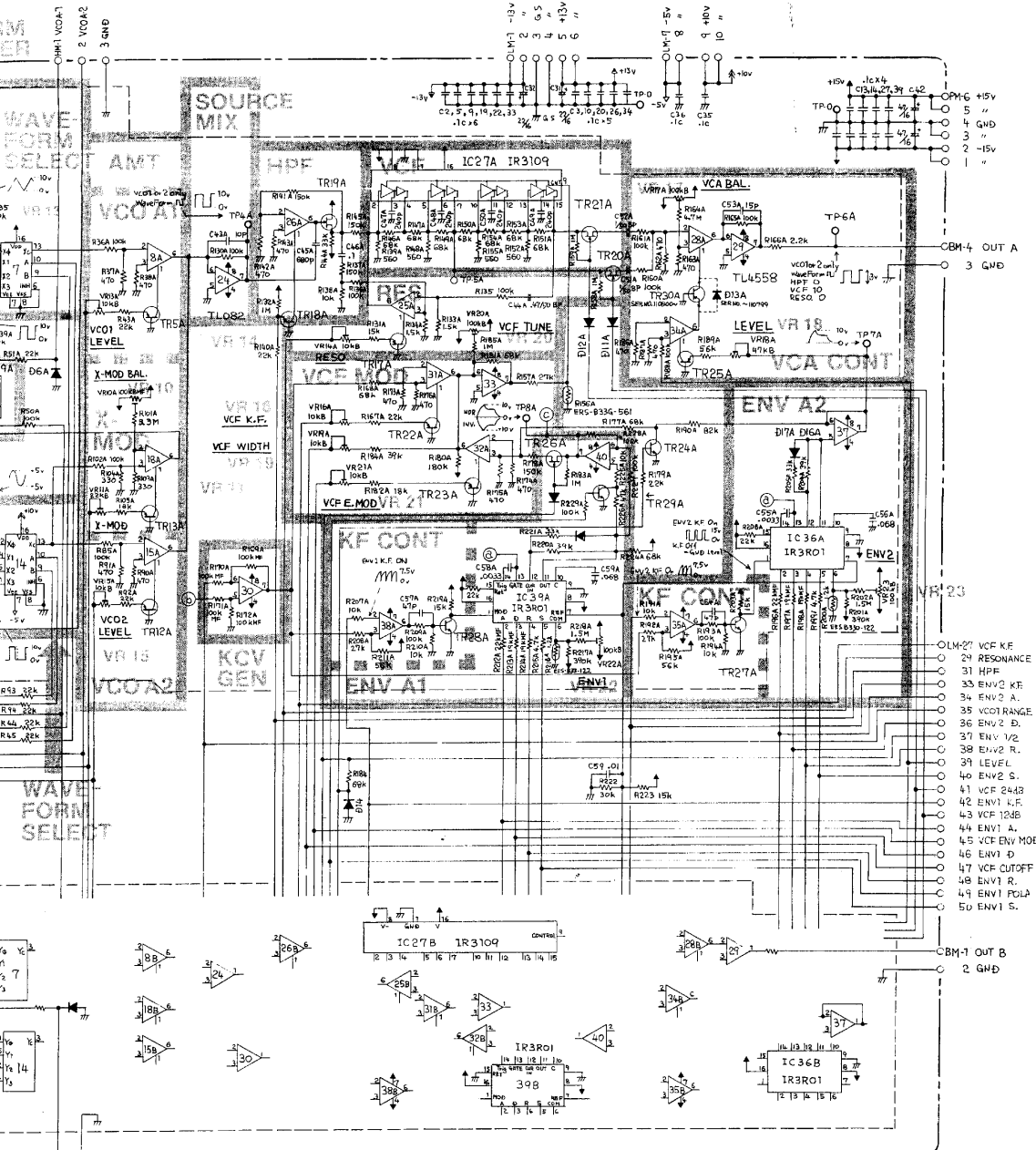


- IC 7A, 1B, 5, 9A, 9B, 19, 21, 30, 33, 37, 40 : 4558
 IC 2, 10 : RC3046
 IC 3A, 3B, 4A, 4B, 11A, 11B, 12A, 12B, 35A, 35B, 38A, 38B : TLO80
 IC 6A, 6B, 13A, 13B, 24 : TLO82
 IC 7, 16 : 4052
 IC 8A, 8B, 15A, 15B, 18A, 18B, 20A, 20B, 22A, 22B, 25A, 25B, 26A, 26B, 28A, 28B, 31A, 31B, 32A, 32B, 34A, 34B : BA662
 IC 16, 17, 23 : 4053
 IC 27A, 27B : IR3109
 IC 29 : TL4558 or NJM459DD
 IC 36A, 36B, 39A, 39B : IR3061

- All PNP TR : 2SA1015-GR
 TR 4A, 4B, 9A, 9B, 11A, 11B : 2SC752-Y
 Other NPN TR : 2C1815-GR
 TR 21, 2B, 8A, 8B : NFB510
 Other FET : 2SK30A-GR
 All Diode : 1S2473

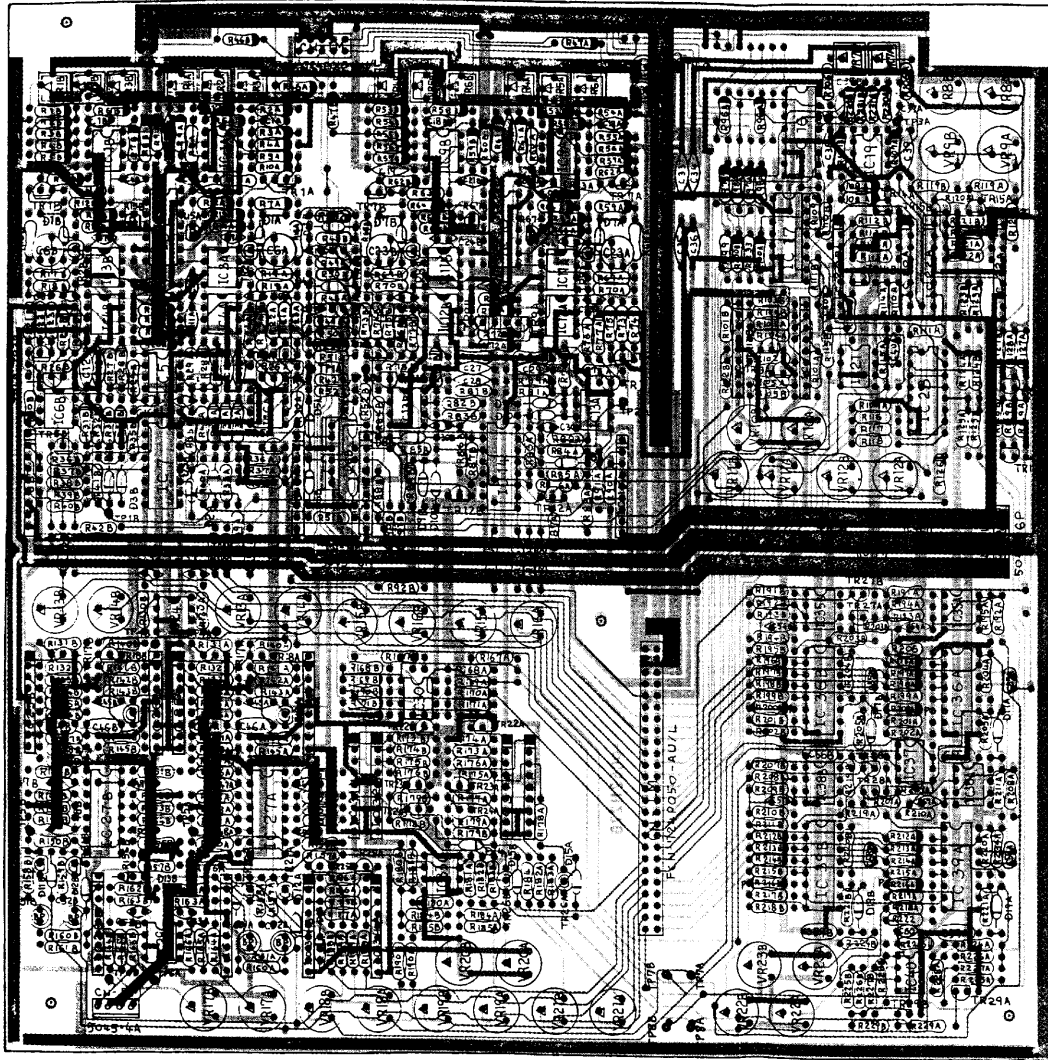
There are two different GND's:
 Highest Ref. Des are IC 40,
 VCOB-1, IHHC-C

MODULE BOARD CIRCUIT DIAGRAM
MODULE BOARD




















There are two different GND lines. Pin 1 is not connected to pin 1 on this PCB.
 Highest Ref. Dex are IC 40, TR 29, D39, C50, R222, VR 23B
 30B 21B 233

A
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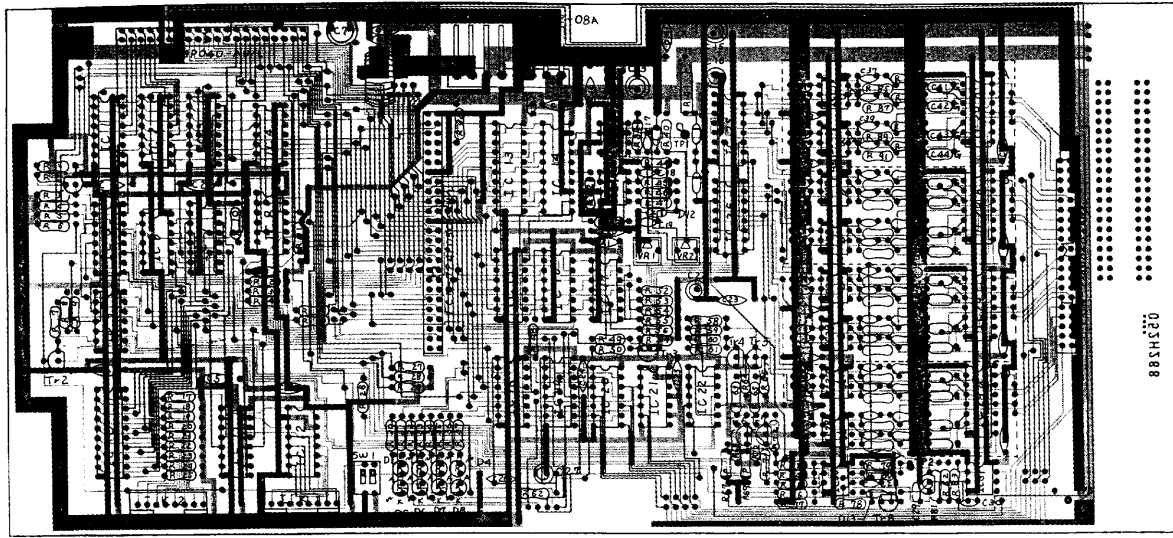


MODULE BOARD
OPH124(149H124)
 (pcb 052H270)

SEE PAGE 48
For SN up to 090599

-  R25G
 selected on slew rate
 TLO80 8PCS
 C82 5PCS
-  carbon R25
 metal film RB25FX
-  POSISTERS: C33G561
-  polysty: 5P102
-  25A1015-GR
-  25C: 215-GR
-  25C152-Y
-  25K30A-GR
-  NF510
-  152473
-  BA662
-  ET-6P
 A or B
 selected on VF (Gm)
 replacement should be
 of the existing
-  Selected on offset
 10 PCS
 white dot
-  SR19
-  test point LC-28 (TP-4: 400)
-  polystyrene film
-  bi-polar

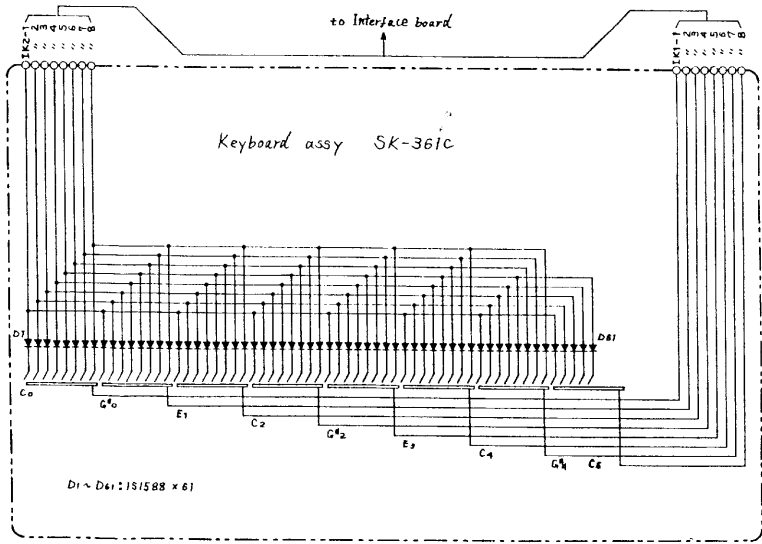
A
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V



See pp. 34-35 for
SN171700 and up

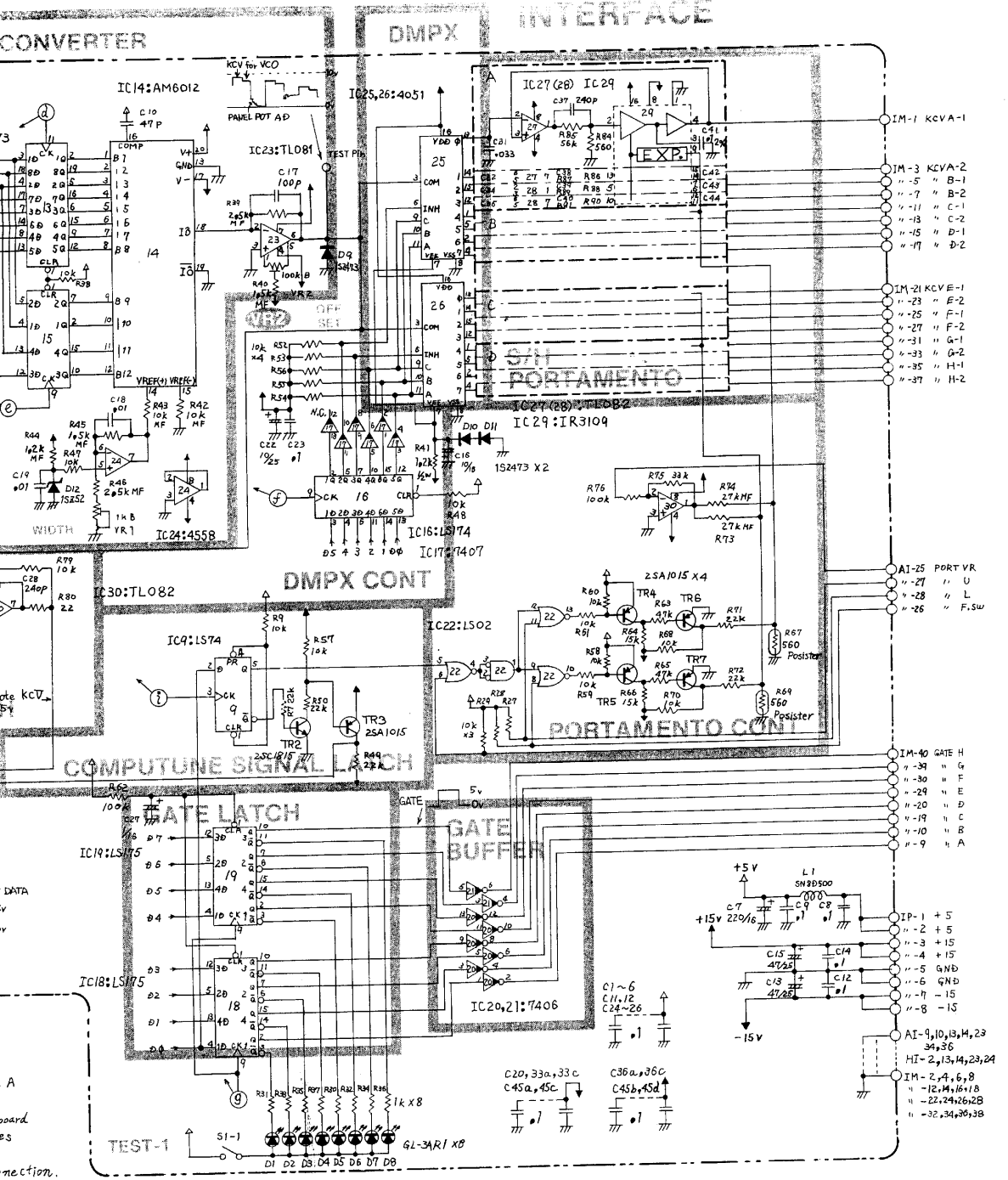
CAUTION
When replacing Interface board bearing
edition no. 052H268 (and below) with PCB
of 052H268 (and above), refer to pp. 34 and
35 for PROMs versions of CPU board.

- R25J
- CR8 25 FX
POD:500N
- ERS-C33G561
- R50J
- ET-6P
- TL082
Selected on cement leakage
- 2SC1015-GR
- 2SA1015-GR
- 2SK30A-GR
- 1S2473
- 1S252
- LED GL-BARI

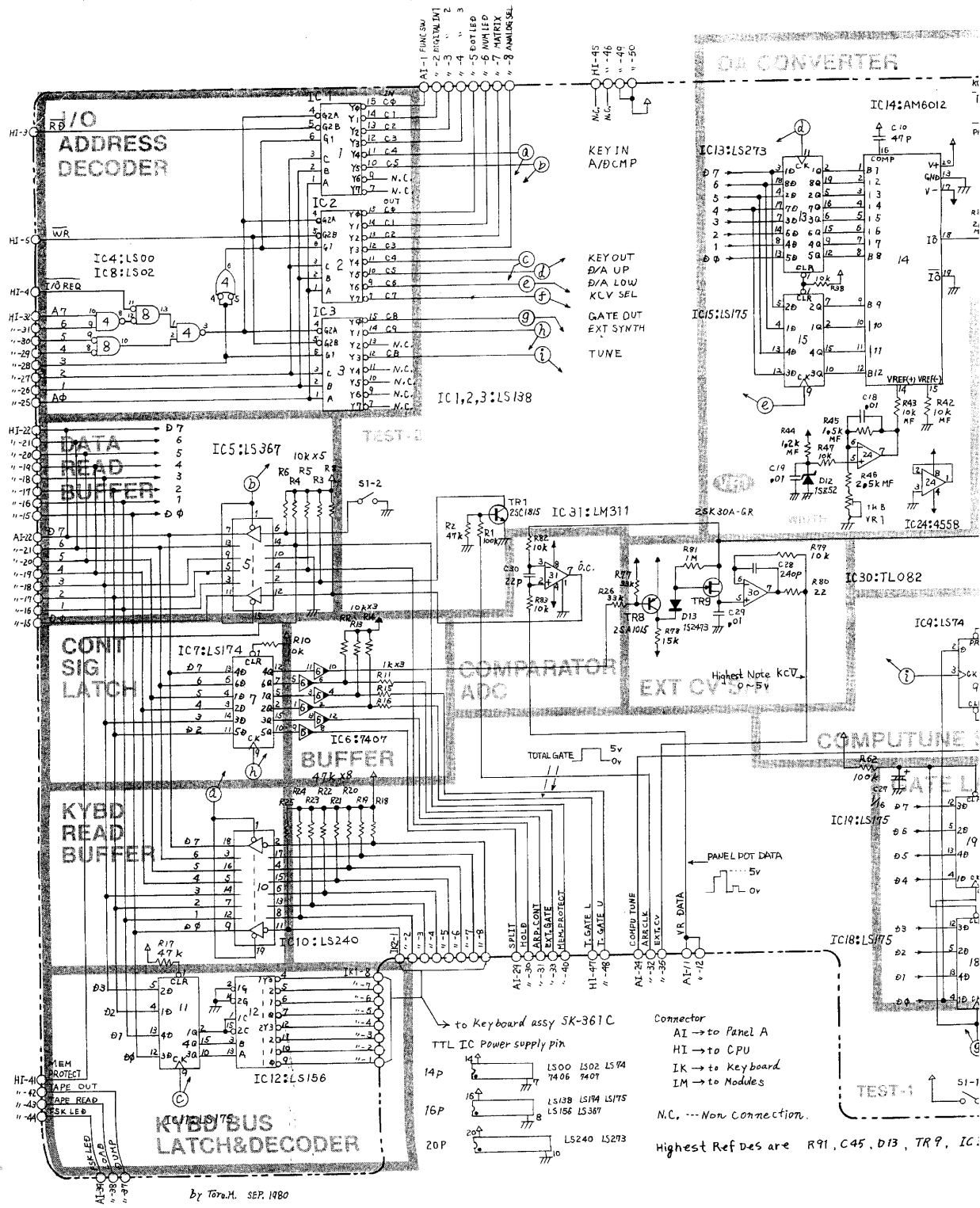


D1 ~ D61: 1S1588 x 61

by TORU.M. SEP.1980



Components are R91, C45, D13, TR9, IC31, VR2, L1, SW1

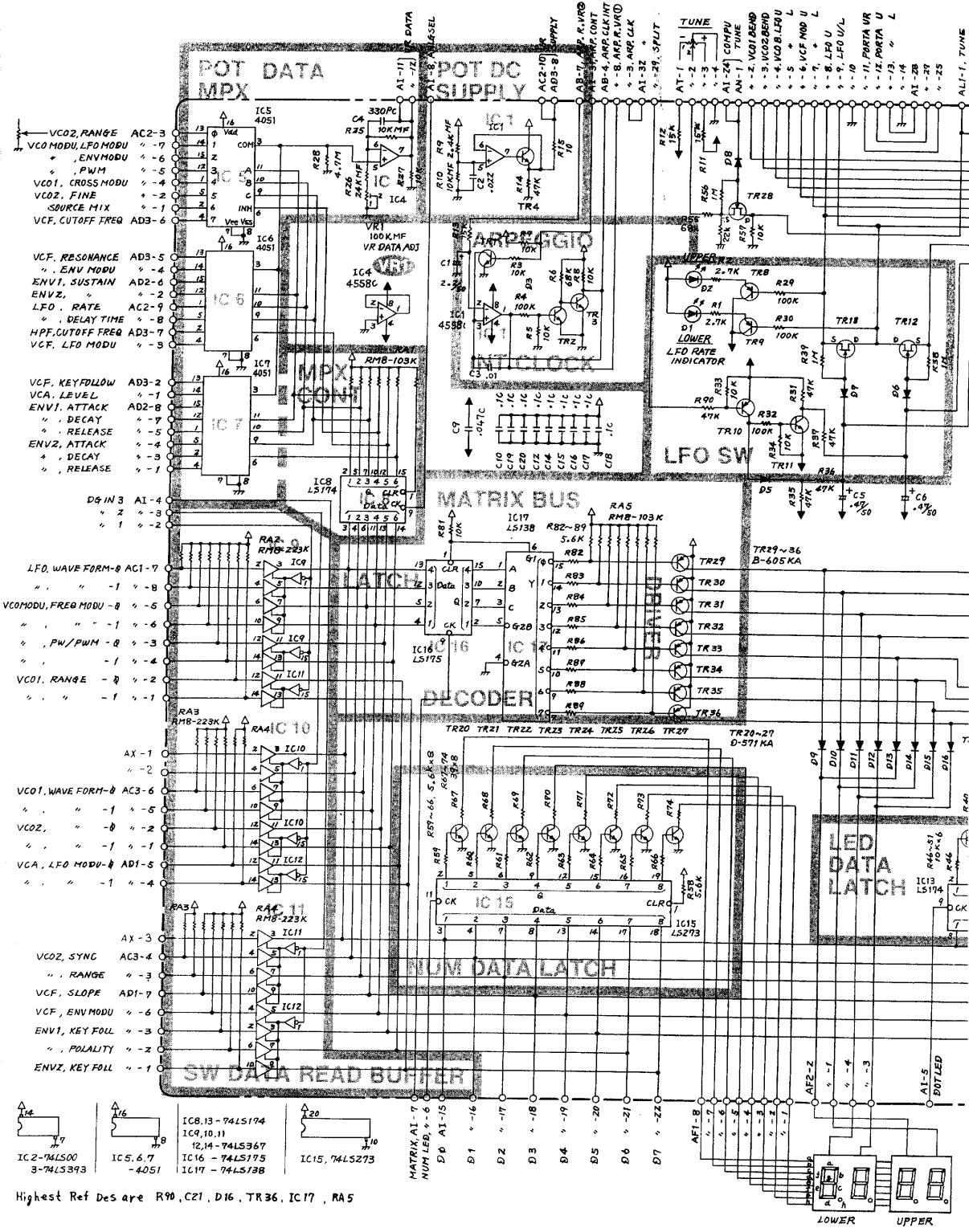


By Tom M. SEP. 1980

- Connector
- AI → to Panel A
 - HI → to CPU
 - IK → to Keyboard
 - IM → to Modules
- N.C. --- Non Connection.
- Highest Ref Des are R91, C45, D13, TR9, IC1

- to Keyboard assy SK-361C
- TTL IC Power supply pin
- 14P → LS00 LS02 LS174 7406 7407
 - 16P → LS138 LS174 LS175 LS156 LS367
 - 20P → LS240 LS273

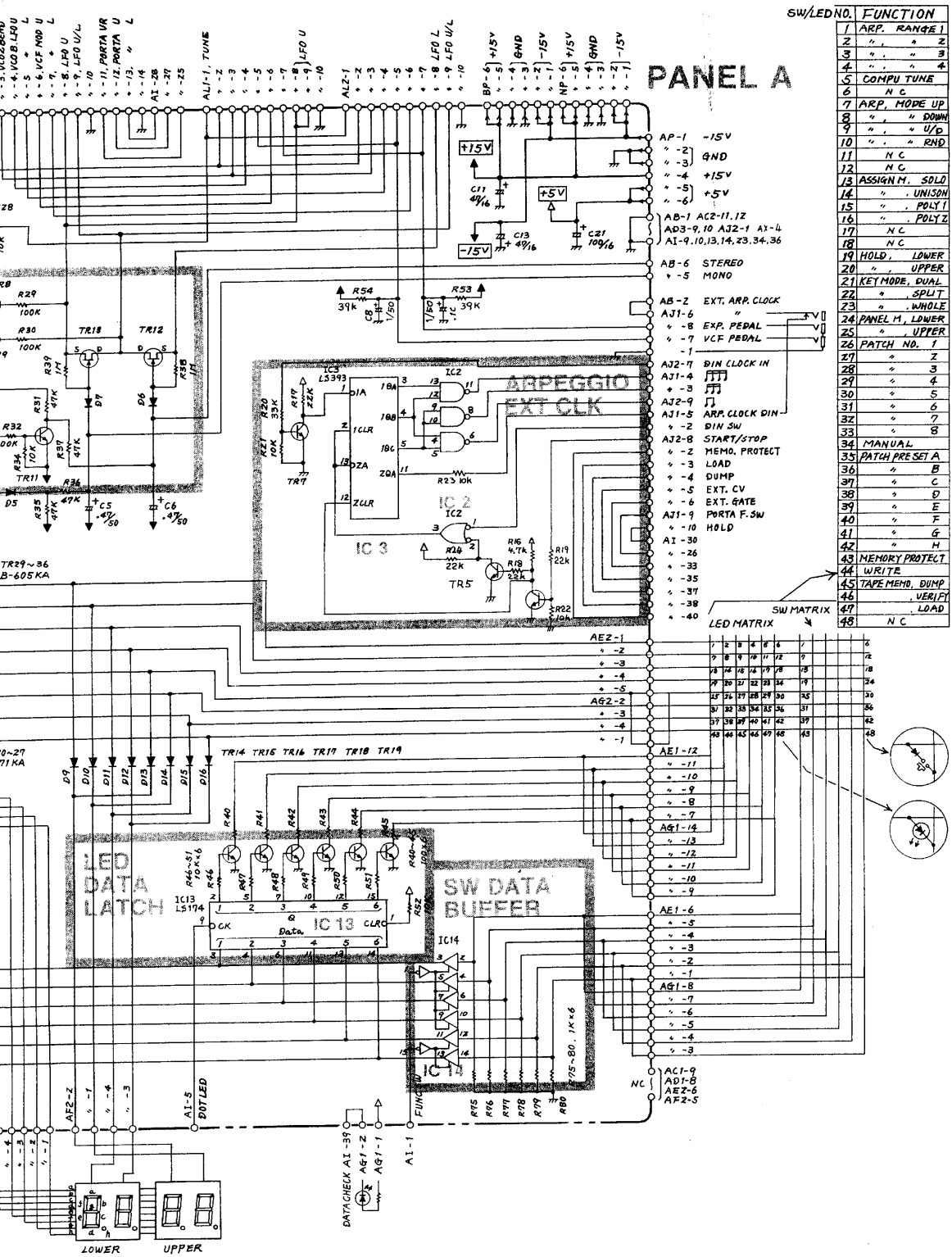
TEST-1



IC2-74LS00 3-74LS393	IC5, 6, 7 -4051	IC8, 13-74LS174 IC4, 10, 11 12, 14-74LS367 IC16-74LS175 IC17-74LS138	IC15, 74LS273
-------------------------	--------------------	--	---------------

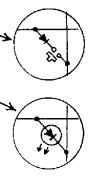
Highest Ref Des are R90, C21, D16, TR36, IC17, RA5

LOWER UPPER









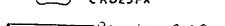



PANEL A

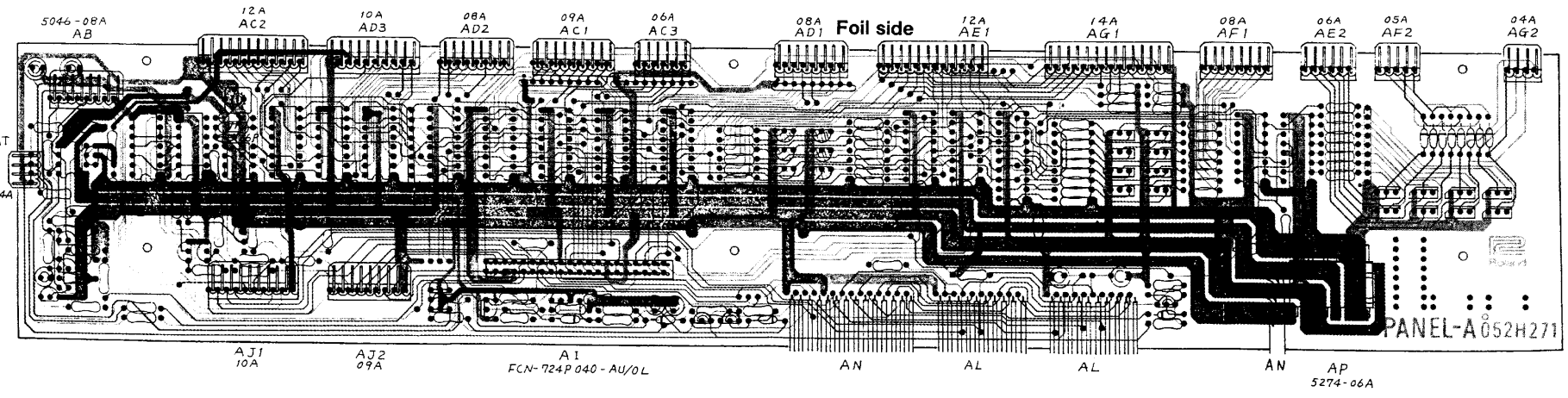
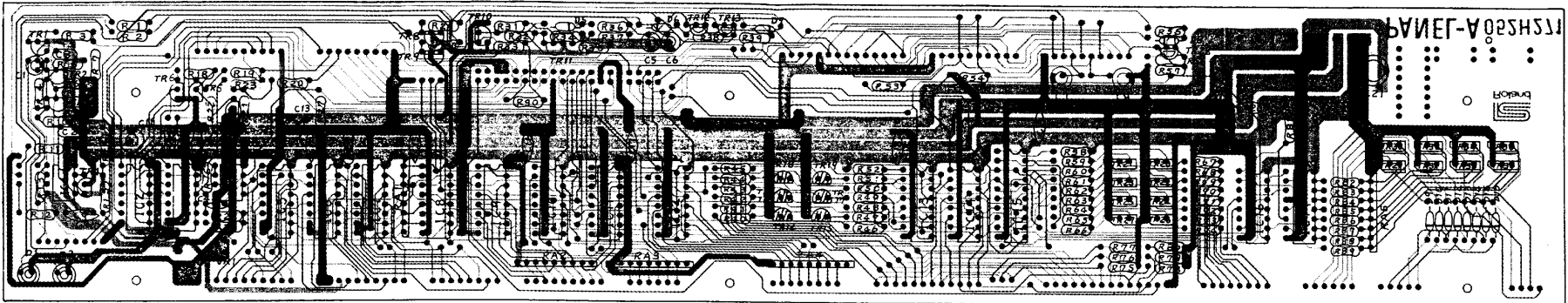
SW/LED NO.	FUNCTION
1	ARP. RANGE 1
2	" " 2
3	" " 3
4	" " 4
5	COMPU TUNE
6	N C
7	ARP. MODE UP
8	" " DOWN
9	" " U/P
10	" " RND
11	N C
12	N C
13	ASSIGN M. SOLD
14	" " UNISON
15	" " POLY 1
16	" " POLY 2
17	N C
18	N C
19	HOLD, LOWER
20	" " UPPER
21	KEY MODE, DUAL
22	" " SPLIT
23	" " WHOLE
24	PANEL M. LOWER
25	" " UPPER
26	PATCH NO. 1
27	" " 2
28	" " 3
29	" " 4
30	" " 5
31	" " 6
32	" " 7
33	" " 8
34	MANUAL
35	PATH PRE SET A
36	" " B
37	" " C
38	" " D
39	" " E
40	" " F
41	" " G
42	" " H
43	MEMORY PROTECT
44	WRITE
45	TAPE MEMO. DUMP
46	VERIFY
47	LOAD
48	N C



PANEL BOARD A OPH125(149H125) (pcb 052H271)

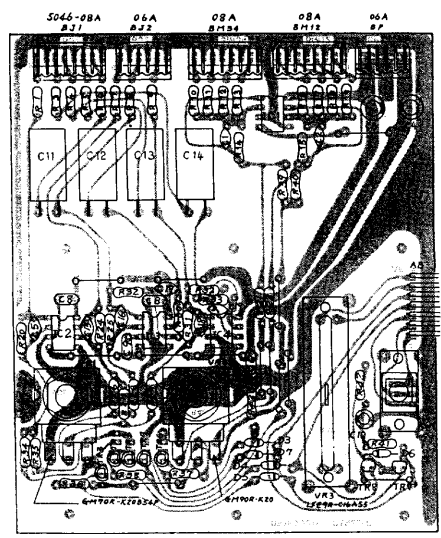
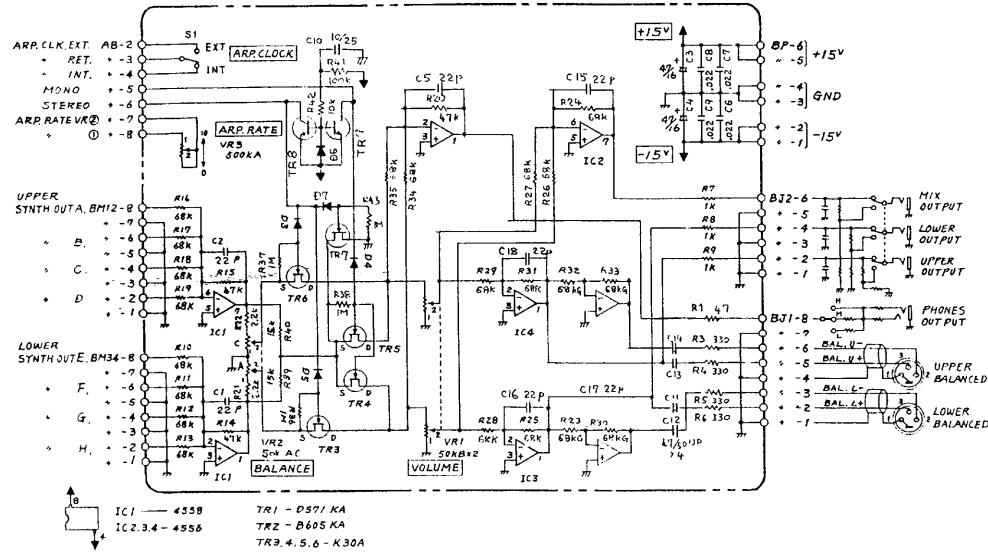
- | | | |
|---|---|--|
|  A1015 Y or GR |  D571 KA |  R25J |
|  C1815 Y or GR |  K30A GR |  CR025FX |
|  C1815 GR |  152473 |  Resistor Array |
|  B605 KA | | |

Component side



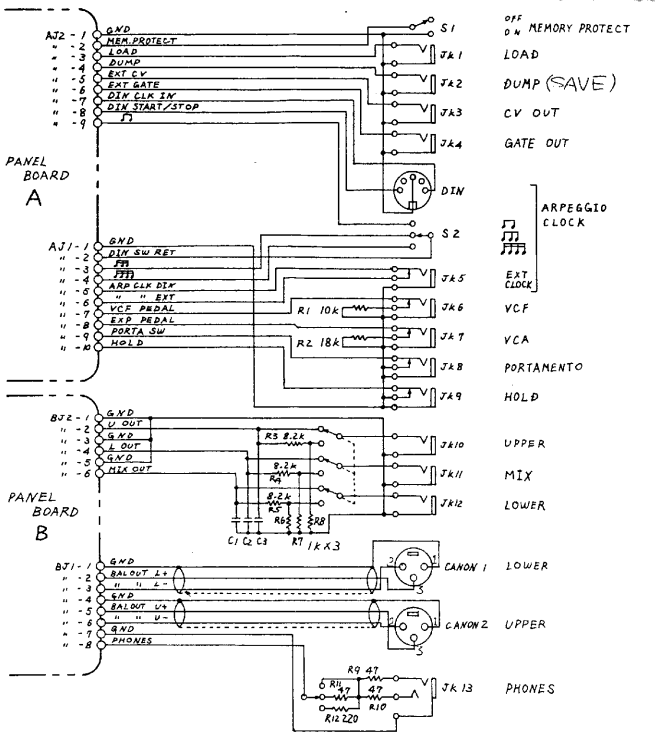
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

A
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C
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F
G
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I
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K
L
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R
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V
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Z

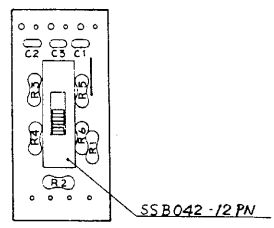


PANEL BOARD B
OPH126(149H126)
(pcb 052H272)

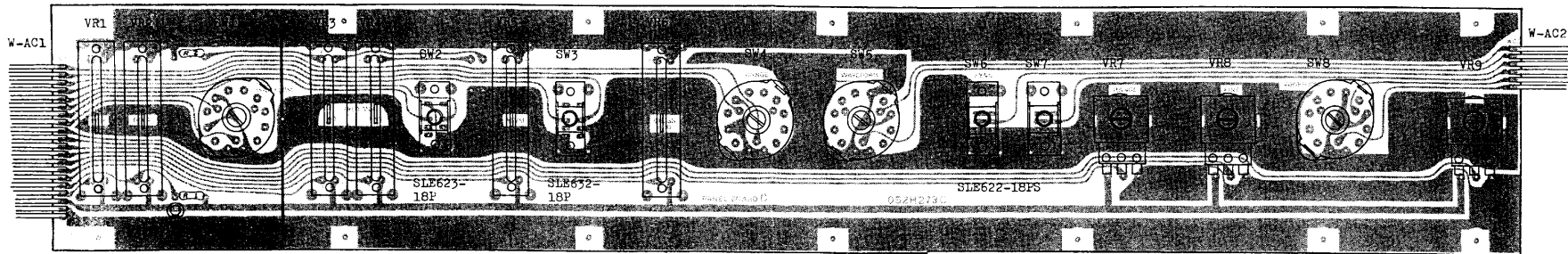
- R25 J
- 1S2473
- 25K30A
- 25C1815 GR



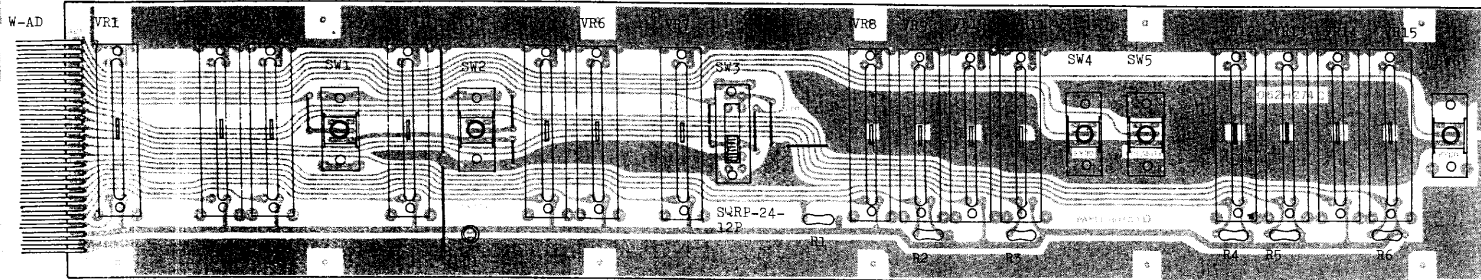
LEVEL SELECT BOARD
OPH139(149H139)
(pcb 052H330)



SSB042 -12 PN

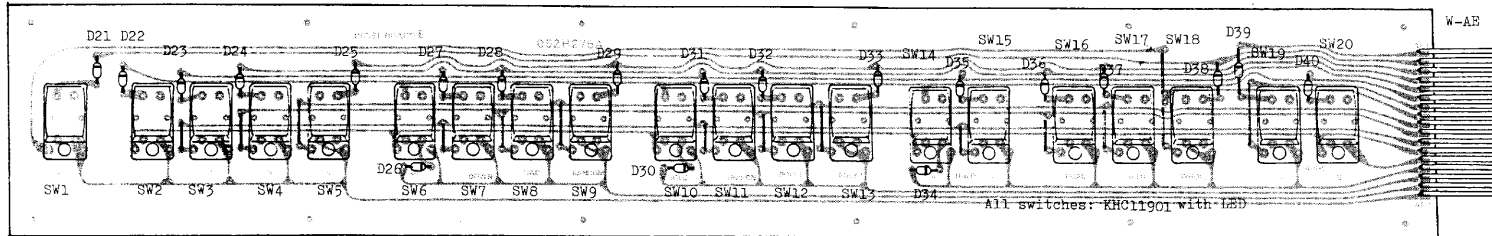


All sliders: LFB9RC16B14 All rotary pots: VM10RK20B14 All rotary switches: SRM1034-K15



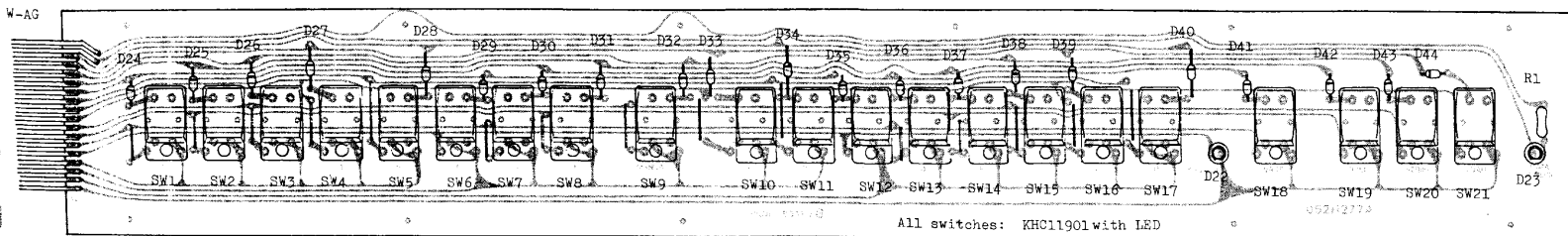
All sliders: LFB9RC16B14 All lever switches: SLE622-18PS

PANEL BOARD D
OPH128(149H128)
(pcb 052H274)
View from foil side



All switches: KHC11901 with LED

PANEL BOARD E
OPH129(149H129)
(pcb 052H275)
View from foil side

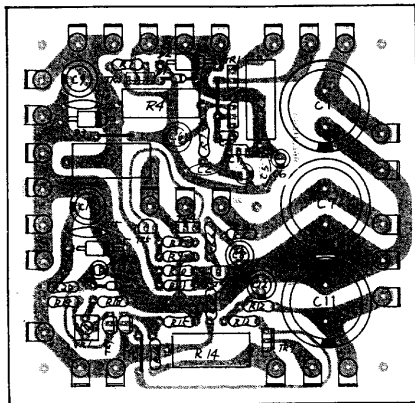


All switches: KHC11901 with LED

PANEL BOARD G
OPH131(149H131)
(pcb 052H277)
View from foil side

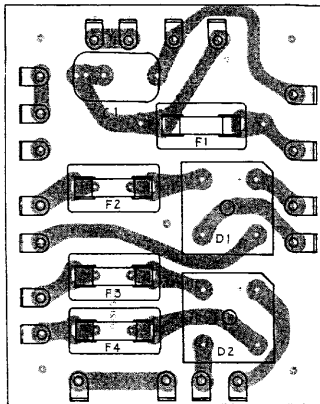
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POWER SUPPLY BOARD A
PSH059(146H059) (pcb 052H279)

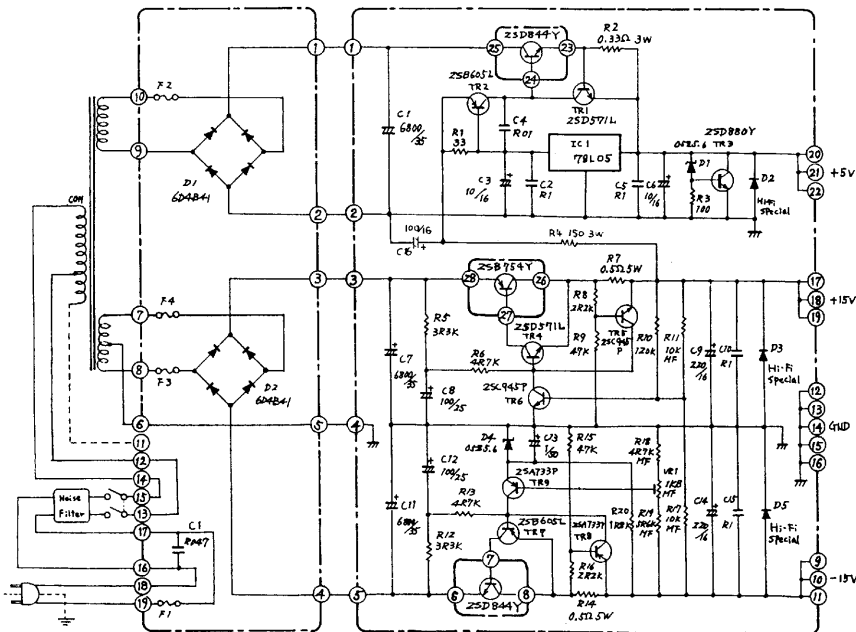


POWER TRANSFORMER SECONDARY RATINGS
+20.5VDC @ 1.3A 4700mfd 1N
+8.5VDC @ 1.3A 4700mfd 1N

POWER SUPPLY BOARD B
PSH061(146H061) 100/117V
PSH062(146H062) 220/240V



100/117V 220/240V
F1 MGP0003 (3.0A) CEE T1.6A
F2 CEE T5.0A
F3 none
F4



This is an 8 bit parallel CPU and is compatible with Z-80A and LH0800A.

- * Instruction sets: 15B
- * Instruction cycle: 1.0µs (4.0MHz)
- * Internal registers: 17
- * address bus: 16 bit
- * Data bus: 8 bit

PIN FUNCTIONS

ADDRESS BUS Transfers 16 bits to memory address decoders (CPU board - IC21, 22 and 23) for controlling the followings:
on CPU board - ROM, CMOS, RAM, N-ch RAM, TAPE and TUNE reading.
on MOD CON board - RAM, UP, LO and VCO select.
Lower 8 bits are transferred to I/O Address decoders (Interface board - IC1, 2, 3, 4 and 8) for controlling the followings:
IN - Function sws, Digital IN (1, 2 and 3), Key IN, A/D.
OUT - Dot LED, Num LED, Matrix, Analog sel, Key out.
D/A Up/Lc, KCV sel, Gate out, EXT synch, Tune.

DATA BUS Used to transfer 8 bit instructions and data between CPU and memories or I/O device.

φ Square wave, 4 Mhz. Derived from X-tal oscillator's 8 Mhz, divided-by-two through frequency divider.

MRQ (Memory Request) Indicates that Address bus holds a valid memory address for a memory read and memory write.

IORQ (I/O Request) Indicates the presence of I/O Device number at pins A6-A7 during I/O write/read cycle.

RD (Memory read) Indicates that CPU wants to read data from memory or I/O device. The addressed memory or I/O device outputs data onto the CPU data bus at positive transition of RD.

WR (Memory write) Indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device which latches the data off of the bus at positive transition of WR.

INT (Interrupt Request) Whenever INT (φ, frequency divided by Counter-2, 1040) is fed to CPU every 1ms via IC26, it accepts INT upon finishing processing job then starts executing Panel LED lighting program, generating INT Acknowledge as an TORQ in M1 cycle.

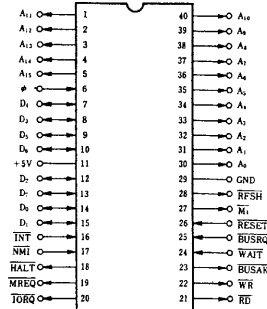
WAIT Lengthens read or write cycle until data on the data bus becomes valid during the presence of address signal for timing CPU access time to memory or I/O device.

RESET Initializes CPU circuits upon power on for the JF-8 or when DC voltages drop below specified value.

µPD780 C/D-1

8 BIT MICROPROCESSOR

(Top View)



REGISTERS

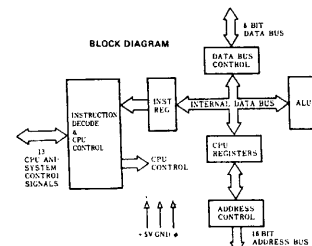
MAIN REG SET				ALTERNATE REG SET			
ACCUMULATOR A	FLAGS F	ACCUMULATOR B	FLAGS G	ACCUMULATOR C	FLAGS H	ACCUMULATOR D	FLAGS I
B	C	B	C				
D	E	D	E				
H	L	M	L				

GENERAL PURPOSE REGISTERS

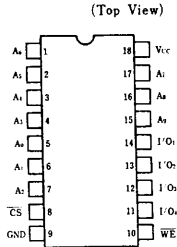
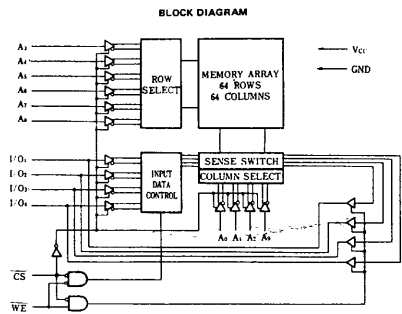
INTERRUPT VECTOR	MEMORY REFRESH
INDEX REGISTER IX	
INDEX REGISTER IY	
STACK POINTER SP	
PROGRAM COUNTER PC	

SPECIAL PURPOSE REGISTERS

BLOCK DIAGRAM

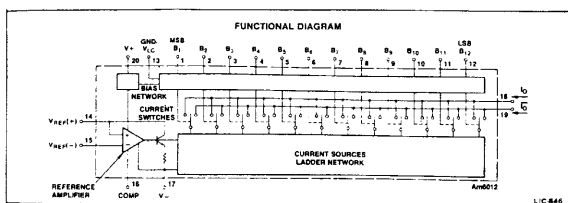
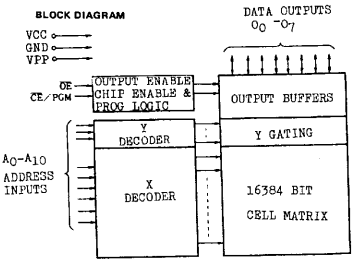
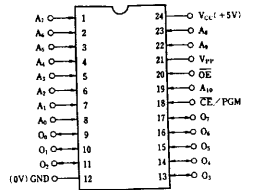


μPD444C
1024 X 4 BIT STATIC RAM CMOS RAM

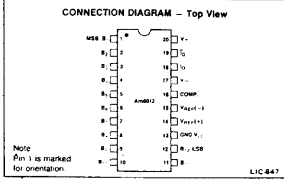


μPD2716D
16K (2K x 8) UV ERASABLE PROM

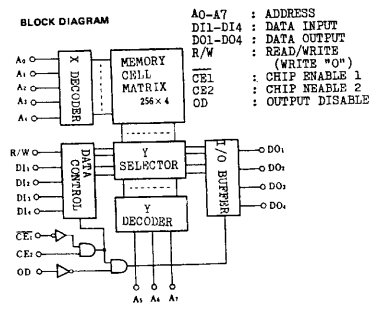
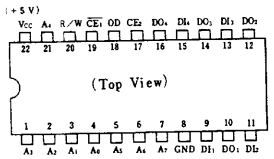
(Top View)



Am6012
12-Bit High-Speed Multiplying D/A Converter

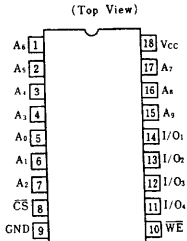
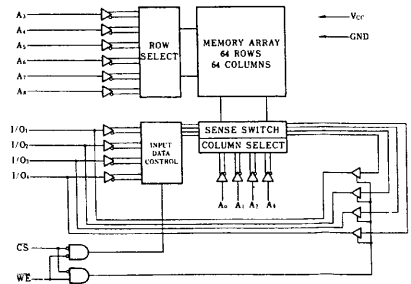


μPD2101ALC
1024 BIT (256x4) STATIC MOS RAM



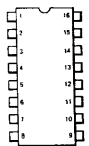
μPD2114LC/D
1024 X 4 BIT STATIC RAM

BLOCK DIAGRAM

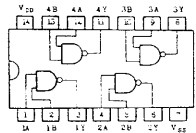


IR3R01

- 1 NODE INPUT
- 2 ATTACK TIME INPUT
- 3 DECAY TIME INPUT
- 4 RELEASE TIME INPUT
- 5 SUSTAIN VOLTAGE INPUT
- 6 COMMON INPUT 0.3V
- 7 REFERENCE VOLTAGE
- 8 V_{EE}
- 9 GROUND
- 10 CAPACITOR
- 11 OUTPUT
- 12 CURRENT INPUT
- 13 GATE INPUT
- 14 TRIGGER INPUT
- 15 RETRIGGER INPUT
- 16 V_{CC}



TC40H000P QUAD 2-INPUT NAND GATE



ADJUSTMENTS

DISASSEMBLY

Follow procedure on page 2. Preparation of a STAY (chain or string) and prop is advisable for a stable top panel rest.

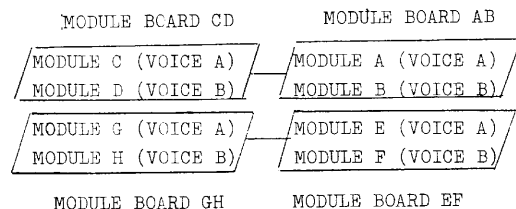
PRECAUTIONS

Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, most circuits are temperature-sensitive.

The adjustments on the JP-8 should not be done more than necessary. Adjustments merely attempted on a particular module (VOICE) might cause sound balance away from entire VOICES and can, in an extreme case, require the same procedures to be done fifteen times for the remainder.

DESIGNATION — TEST POINT, TRIMMER, PCB —

For PCBs that are identical in circuit configuration, most adjustment steps, test points and trimmers do not refer to a particular PCB or module (VOICE), they may be read as ones on a PCB to be adjusted.



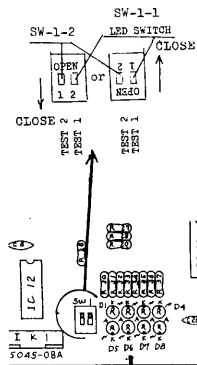
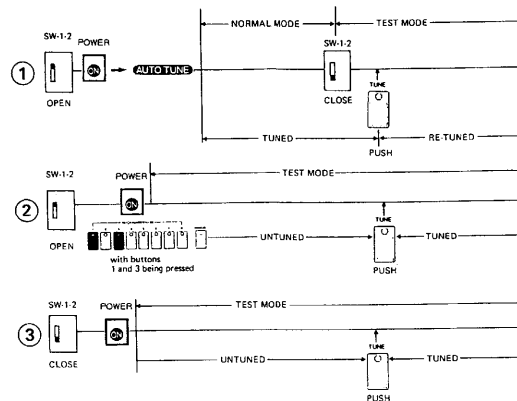
Four module boards, each consisting of two voices, are identical in all aspects, having the same designators with A or B suffix for the same components of two VOICES, e.g. VR1A (VOICE A) and VR1B (VOICE B). Note that each voice contains two VCOs, VCO-1 and VCO-2.

ADJUSTING ORDER

The adjustments proceed from paragraph 1, DC Supply assuming that the JP-8 is completely unadjusted. When adjusting a specific section, begin with lower numbered para. in the relative adjustment section, e.g. first No. 7 BAL, then, No. 8 DEPTH, as directed.

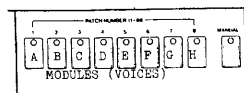
TEST MODES

Adjustments on the JP-8 proceed in TEST MODEs. Although three TEST MODEs are available for the adjustments, TEST MODE (3) is chosen in this manual unless otherwise specified. (For more details refer to TEST MODE in Circuit Description — separate copy.)



TEST LEDs (INTERFACE BOARD)

MODULES: A B C D
LEDs:
MODULES: E F G H



Below confines description to the point inevitably necessary for performing the adjustments.

To put the JP-8 into TEST MODE 3

See figure above 3. With power off, throw SW-1-2 on Interface board from OPEN to TEST-1 or -2 (on some early models the switch is oriented opposite, so are labels TEST-1/2 on PCB, left hand one is always SW-1-2 and OPEN position is at label "OPEN" on the SW).

In the TEST MODE 3

The JP-8 has the following functions that are different from those in NORMAL MODE:

All VCOs are uncompu-tuned, i.e. their pitches are left deviated slightly until "TUNE" is pressed.

- * Among key assignments, POLY-1 only changes assigning order — tapping single key (same key) will assign modules from A to H one by one, repeating the order. This is convenient in comparing 8 modules sounds (timbre, pitch, etc.) sequentially at a note.
- * Computer provides FSK adjustment (para. 26) program and outputs test signal at SAVE (DUMP) jack when VERIFY is pressed.
- * Integrated PATCH NUMBER LEDs serve as module (VCO) indicator for visible checking, identifying VCO(s) being directed by key(s) has been depressed or being held down.

SW-1-1, LED switch, in close position, allows LEDs (TEST LED) located right to it to be energized regardless of MODE (NORMAL or TEST) when gate signals are fed to them individually. The LEDs function as assignment indicator just as Patch Number LEDs do. Test LEDs find extended application for learning and checking the assignments varying to MODEs (KEY, PANEL and ASSIGN) in Normal mode.

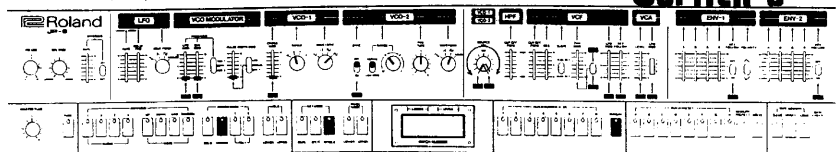
Patch Number LEDs are lit automatically in sequence immediately after TUNE is touched, representing module A VCO-1 (leftmost LED), A VCO-2 (No.2 LED) and so on; the first cycle for Upper modules' and the second for Lower. Their lighting period is proportional to degree of VCO detune from standard pitches. An LED staying on and won't pass illumination to the next one claims checking of its mated VCO having been far out of computer controllable range.

TEST MODEs 2 and 3 are identical to each other in function, but any panel disassembly is required for mode 2 if the purpose is only to check Key Assignment or VCO detune.

FOR SATISFACTORY SERVICE WORK

1. Dump user's preset memory on tape before attempting adjustments and troubleshooting.
2. If TUNE was pressed in previous adjustments, be sure to power off and on the JP-8 before making adjustment which must be done without compu-tune.
3. Plural keying and miskeying will disorder key assignment sequence. Push HOLD or ASSIGN MODE to off and again to on, as appropriate, to restore the order. Use monitor amp to detect erroneous key assignment that LED does not distinguish.
4. Make a practice of pushing MANUAL after changing PANEL MODEs.
5. Restore SW-1-1 and SW-1-2 to OPEN and load back the data on tape before return the unit to the customer.

12. VCO LEVEL
MODULE (MOD)



See appendices for adjustment locations and glossary.

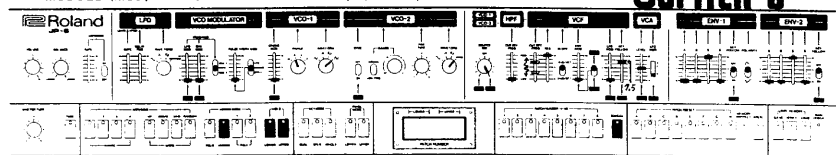
1. Connect scope to MOD TP-4.

CAUTION On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

2. Press A2 key, adjust VR13 for 10V p-p reading.
3. Rotate SOURCE MIX to VCO-2 and adjust VR15 for 10V p-p.

13. VCF KEY FOLLOWER

MODULE (MOD) MODULE CONTROLLER (MOD CON)



See appendices for adjustment locations and glossary.

This adjustment must be followed by para. 14-17.

CAUTION

On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166 lead.
3. Turn MOD VR14 fully clockwise. The VCFs resonate.
4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (across the graticules, same for the rest para.) MOD VR20 may be used for fine adjustment.

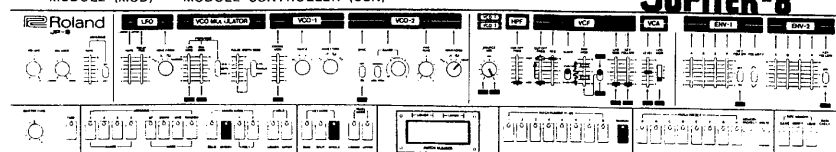
5. Press C4 key, adjust VR16 to display 4 complete cycles.

NOTE:

VR14 and VR20 will be readjusted in later para.

14. VCF WIDTH

MODULE (MOD) MODULE CONTROLLER (CON)



Para. 13-17 must be performed in sequence.

On JP-8's S/N **0600 and subsequent, read figures in parentheses.

1. With scope to MOD TP-6 set timebase to 1ms (2ms)/div.
2. press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.
3. Set CO FREQ to 10, scope timebase to 5μs/div (20μs/div). Adjust VR19 to display one complete cycle (5 cycles).

Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.

1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.
2. Reset VCF ENV MOD to 10, timebase to 50μs/div. Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change setup in para. 15 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 - 4); scope to MOD TP-6 with A-442 reference fed to H IN.

1. Press a key, adjust VR20 for 1:1 Lissajous.

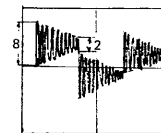
17. RESONANCE LEVEL

MODULE (MOD)

Para. 13-17 must be performed in sequence.

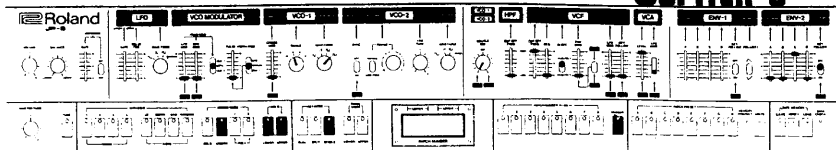
Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.

1. Press A2 key (S/N **0600 - E3 key), adjust VR14 for the figure:



18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)



See appendices for adjustment locations and glossary.

Although CON VR5 is included in part-1, the trimpot is replaced by 10k resistor on later products. When adjusting MOD replacement, ignore VR5 trimming, following Part 2.

Connect scope to TP-6 or R166 lead.

PART 1

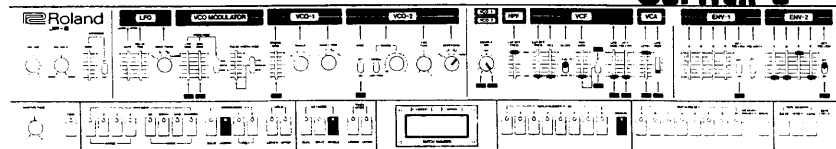
1. Set MOD VR18 wiper to midpoint.
2. Press C2 key and adjust CON VR5 for 3V p-p.
3. Adjust VR18 of the remainder Voices for 3V p-p.

PART 2

1. Press C2 key and adjust VR18 for 3V p-p.

19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

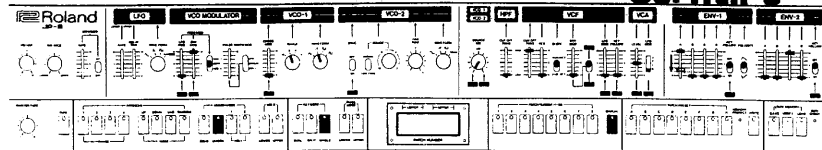


See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

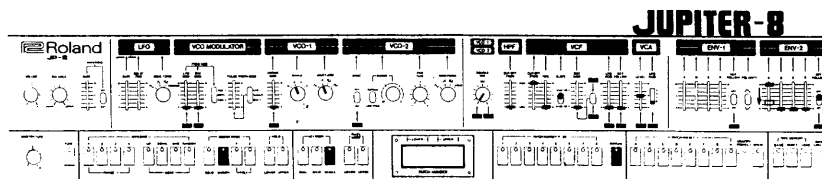
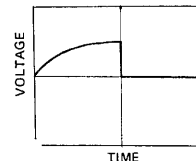


See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICES' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

ENV-1

1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
3. Switch scope timebase to 20ms/div. Trigger scope from TR16 collector of any module.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI1 or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.

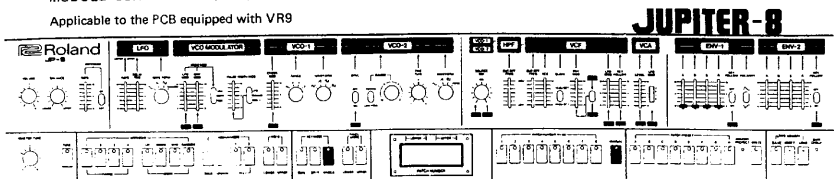


ENV-2

The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.

7-1. ENV-1 S OFFSET
MODULE CONTROLLER (CON)

Applicable to the PCB equipped with VR9

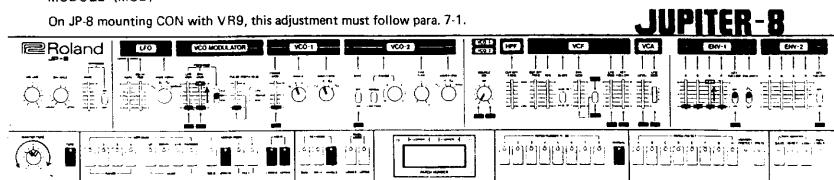


This adjustment must be followed by para. 7. See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-7.
Set scope V to 20mV/div.
2. Adjust CON VR9 for 0V reading.

7. VCO ENV MOD BAL
MODULE (MOD)

On JP-8 mounting CON with VR9, this adjustment must follow para. 7-1.



See appendices for adjustment locations and glossary.

1. Push TUNE.
2. Connect scope to MOD TP-4 with A-442 reference to H IN.
3. Press A2 key, adjust MASTER TUNE for still Lissajous.
4. Slide MOD ENV up to 10. Without additional keying, adjust MOD VR8 for still Lissajous. (Frequency is same as in step 3.)

8. VCO ENV MOD DEPTH
MODULE (MOD)

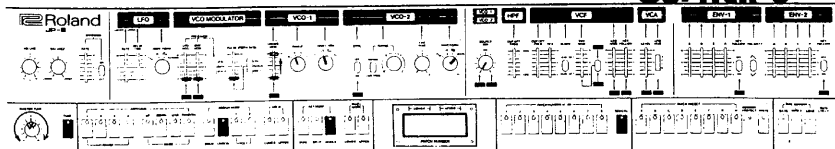
This adjustment must follow para. 7. See appendices for adjustment locations and glossary.

Change from para. 7 setup: ENV-1 S to 10; VCO-1 to 2; VCO MOD ENV to 0.

The adjustment sets maximum voltage of modulating waveform to the value by which VCO's can be shifted within a 3-octave range.

1. Press A0 key, adjust MASTER TUNE for motionless Lissajous.
2. Set VCO-1 to 16; VCO MOD ENV to 10. Leaving A0 key open, adjust MOD VR9 for the same waveform as in step 1.

9. VCO CROSS MOD BALANCE (X-MOD)
MODULE (MOD) MODULE CONTROLLER (CON)



This adjustment must be followed by para. 10. See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 with A-442 reference fed to H IN. Place a ground to CON TP-4 or D-20. Push TUNE.
2. Press A2 key, adjust MASTER TUNE for still Lissajous.
3. Leaving A2 key open, set VCO-1 CROSS MOD to 10. Adjust MOD VR10 for the same Lissajous displayed in step 2.

10. VCO CROSS MOD DEPTH (X-MOD LEVEL)
MODULE (MOD) MODULE CONTROLLER (CON)

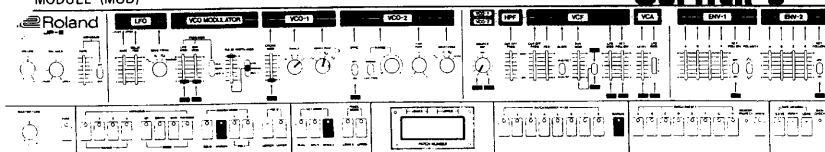
This adjustment must follow para. 9. See appendices for adjustment locations and glossary.

The adjustment sets modulating voltage to the value by which VCO-1 frequency is shifted by 3 octaves when CROSS MOD is set at 5, and VCO-1 RANGE at 2.

Change from para. 9 setup: VCO-1 CROSS MOD to 5; VCO-2 SYNC to on; VCO-2 RANGE to LOW FREQ.

1. Press A0 key, adjust MASTER TUNE so that Lissajous is 1:1.
2. Switch VCO-2 WAVE to square; VCO-1 to 16; Adjust MOD VR11 to display Lissajous observed in step 1.

11. PULSE WIDTH MOD LEVEL (P.W.M.)
MODULE (MOD)

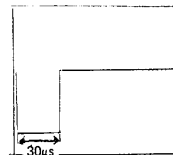


On JP-8's S/N **0600 and subsequent, waveform is up side down.

See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 or R130 lead. Trigger on the negative edge (positive S/N **0600).
2. Press C2 key, adjust MOD VR12 for 30μs space width.

NOTE:
VR12's interact to each other. Check other voices for mark/space ratio. Readjust as necessary.

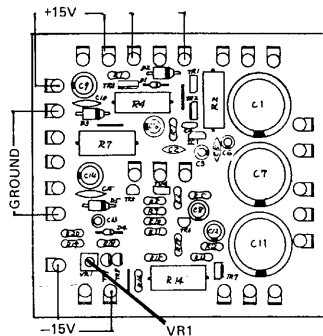


BEFORE STARTING ADJUSTMENTS

ALLOW AT LEAST 30 MINUTES FOR WARUP PERIOD

**1. DC SUPPLY
POWER SUPPLY BOARD**

1. Connect Digital voltmeter (DVM) to -15V (terminal 9, 10, 11).
2. Adjust VR1 for -15V±10mV reading.
3. +15V should be +15V±500mV.
4. +5V should be 5V±400mV.



**2. DC SUPPLY (VCO)
MODULE. MODULE CONTROLLER**

See appendices for adjustment locations and glossary.

MODs A, B, C and D

1. Connect DVM to MOD AB IC1 pin 4 (-VDD).
2. Adjust upper CON VR4 for -13V±5mV.
3. IC1 pin 8 should read -13V±200mV.

MODs E, F, G and H

1. Disconnect flatcables at upper CON LM1 and HL. Observe the note in CON Layout, appendix.
2. Perform step 1-3 above for lower PCBs.

**3. PANEL POTs VOLTAGES
INTERFACE (INT) PANEL BOARD A**

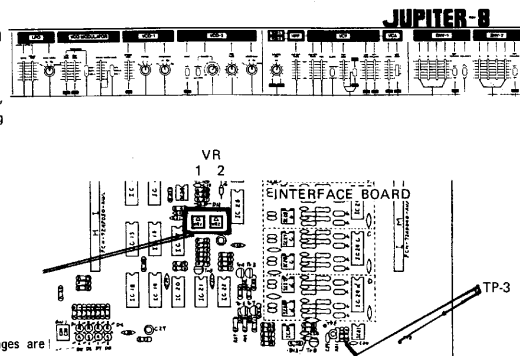
See appendices for locations and glossary.

1. Connect DVM to INT TP-3 or R83 (10k) lead facing outside. (See Fig. below right.)
2. Depress MANUAL.
3. Turn all the pots on the panel illustrated fully cw, or to 10. Incomplete settings result in a fluctuating reading or dips on a screen if observed with scope.
4. Set VR1 (Panel board A) for +5V±2mV.

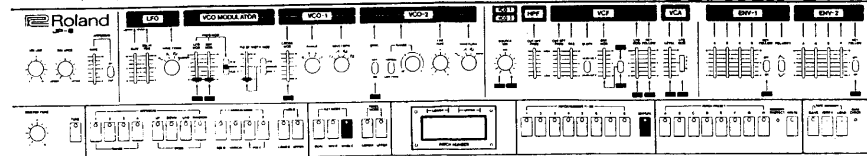
**4. DAC
INTERFACE (INT)**

See appendix for glossary.

1. Connect DVM to OUTPUT CV jack.
2. Press KEY MODE WHOLE.
3. Press C0 key, adjust VR2 for 0.000V reading.
4. Press C5 key, adjust VR1 for 5.000V reading.
5. Check C0-C5 keys for scaling, that those voltages are 1V/oct increments ±2mV.



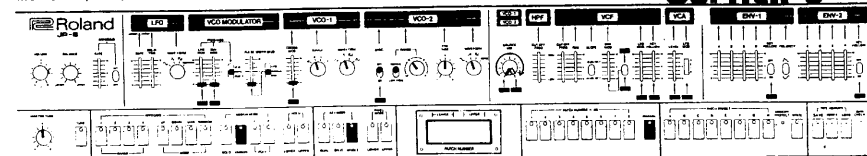
**5. VCO MOD BAL
MODULE (MOD)**



See appendices for adjustment locations and glossary.

1. Connect DVM to MOD TP-3 or R107 lead.
2. Adjust MOD VR7 for 0.000V reading.

**6. VCO TUNE
MODULE (MOD)**



See appendices for adjustment locations and glossary.

Compu-tuned VCO needs to be re-calibrated only if it or associated components have been replaced. If a VCO is excessively out of tune right after compu-tune, first check MOD BAL, para. 5 and KCV OUT (INT terminals IM-1, IM-3, etc.) for voltage. Seconds, isolate possible causes before attempting VCO adjustments.

As is usual with tuning, several instruments may be used for determining frequency. The calibration proceeds by Lissajous figures with A-442 reference fed to scope's horizontal input.

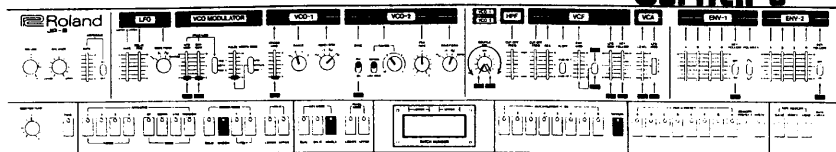
1. Connect scope to MOD TP-4 or R130 lead.
2. Turn SOURCE MIX fully to VCO-1 or 2 accordingly.

NOTE:

Make sure that the JP-8 is in the test mode without initially compu-tuned upon power on. To ensure this, turn power off and on. Then, push UNISON, etc. See "TEST MODE" on the first page of this section.

3. Press A3 key, adjust trimpot T for 884Hz.
4. Press A1 key, adjust trimpot W for 221Hz.
5. Repeat steps 3-4 until waveforms are stationary on both keys.
6. With RANGE set in 2', press A3 key and adjust L for 3536Hz.
7. These trims interact to each other, repeat steps 3-6 until three notes are on the right frequency.

12. VCO LEVEL
MODULE (MOD)



See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4.

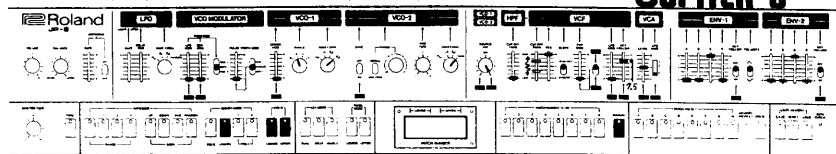
CAUTION On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

2. Press A2 key, adjust VR13 for 10V p-p reading.

3. Rotate SOURCE MIX to VCO-2 and adjust VR15 for 10V p-p.

13. VCF KEY FOLLOWER

MODULE (MOD) MODULE CONTROLLER (MOD CON)



See appendices for adjustment locations and glossary.

This adjustment must be followed by para. 14-17.

CAUTION

On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

1. Place ground to CON TP-4 or D20 cathode.

2. Connect scope to MOD TP-6 or R166 lead.

3. Turn MOD VR14 fully clockwise. The VCFs resonate.

4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (across the graticules, same for the rest para.) MOD VR20 may be used for fine adjustment.

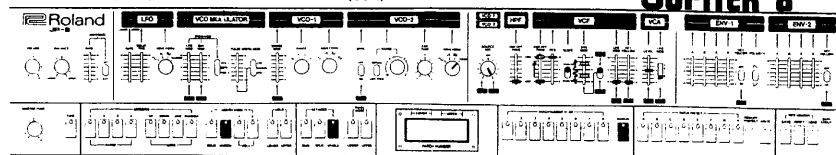
5. Press C4 key, adjust VR16 to display 4 complete cycles.

NOTE:

VR14 and VR20 will be readjusted in later para.

14. VCF WIDTH

MODULE (MOD) MODULE CONTROLLER (CON)



Para. 13-17 must be performed in sequence.

On JP-8's S/N **0600 and subsequent, read figures in parentheses.

1. With scope to MOD TP-6 set timebase to 1ms (2ms)/div.

2. Press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.

3. Set CO FREQ to 10, scope timebase to 5μs/div (20μs/div). Adjust VR19 to display one complete cycle (5 cycles).

Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.

1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.

2. Reset VCF ENV MOD to 10, timebase to 50μs/div. Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change setup in para. 15 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 - 4); scope to MOD TP-6 with A-442 reference fed to H IN.

1. Press a key, adjust VR20 for 1:1 Lissajous.

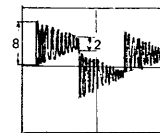
17. RESONANCE LEVEL

MODULE (MOD)

Para. 13-17 must be performed in sequence.

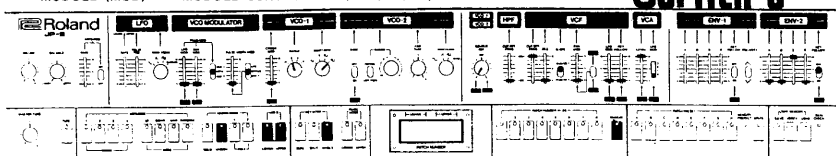
Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.

1. Press A2 key (S/N **0600 - E3 key), adjust VR14 for the figure:



18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)



See appendices for adjustment locations and glossary.

Although CON VR5 is included in part 1, the trimpot is replaced by 10k resistor on later products. When adjusting MOD replacement, ignore VR5 trimming, following Part 2.

Connect scope to TP-6 or R166 lead.

PART 1

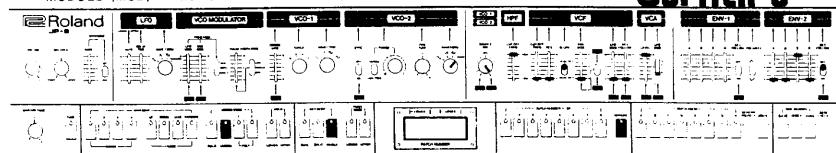
1. Set MOD VR18 wiper to midpoint.
2. Press C2 key and adjust CON VR5 for 3V p-p.
3. Adjust VR18 of the remainder Voices for 3V p-p.

PART 2

1. Press C2 key and adjust VR18 for 3V p-p.

19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

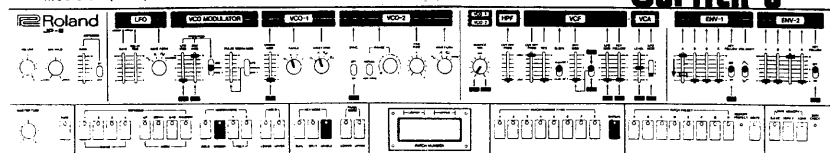


See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

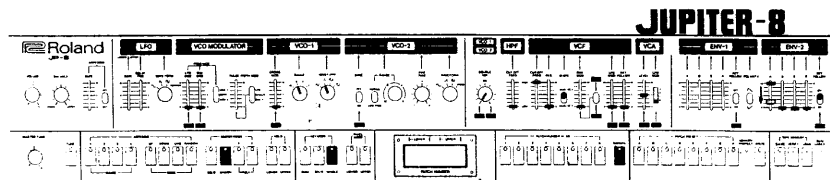
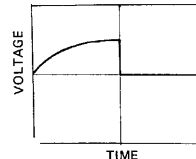


See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICES' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

ENV-1

1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
3. Switch scope timebase to 20ms/div. Trigger scope from TR16 collector of any module.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.

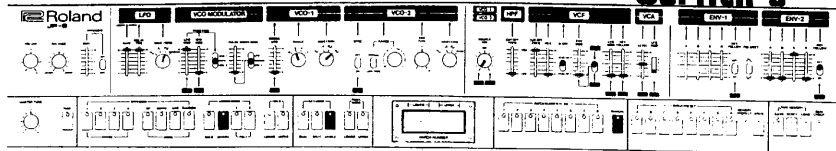


ENV-2

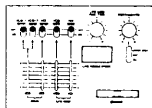
The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.

21. LFO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)



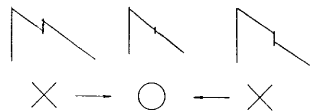
JUPITER-8



See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-5 Or R59 lead. Set timebase to 10ms/div.

2. Adjust CON VR3 to display exactly 3 complete cycles on the scope.



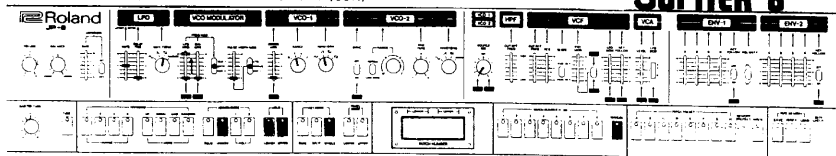
3. Adjust CON VR2 for slope straightness as shown in Fig. right.

4. Shift scope to TP-4 of (Upper - MOD A; Lower - MOD E).

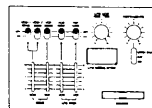
Repeatedly holding a key, adjust CON VR8 so that VCO becomes being modulated approx. 4 sec after the key first depressed.

22. VCO LEO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)



JUPITER-8



See appendices for adjustment locations and glossary.

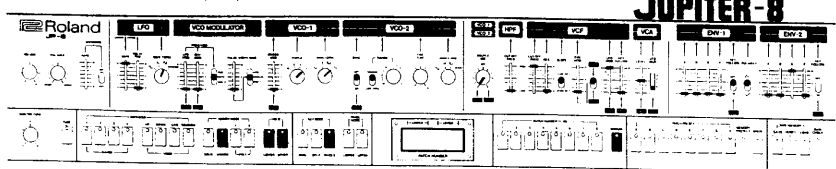
1. Connect scope (with A-442 into H IN) to TP-4 of (Upper-MOD A; Lower - MOD E).

2. Press A2 key, adjust MASTER TUNE for 1:1 Lissajous.

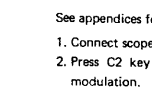
3. Set VCO LFO MOD to 10. Lissajous ratio is now changing up and down in sympathy with LFO rate. Adjust CON VR6 so that Lissajous becomes 2:1 at the highest pitch. Note that LFO modulated VCO swing equals 2 oct's.

23. VCF LFO MOD LEVEL

MODULE CONTROLLER (CON)



JUPITER-8



See appendices for adjustment locations and glossary.

1. Connect scope to TP-6 of (Upper - MOD A; Lower - MOD E).

2. Press C2 key (S/N **0600 - C4 key), adjust CON VR7 for 50 percentage modulation.



24. NOISE

MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.

1. Switch VCO 2 RANGE to NORMAL. Connect scope to CON TP-4.

2. Adjust CON VR1 so that dense signal peaks are approx. 5V p-p.

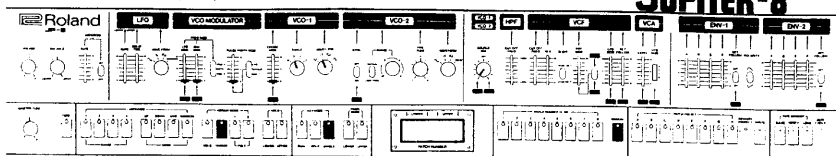
3. Switch RANGE to LOW FREQ, check peaks for clip.

NORMAL RANGE LOW FREQ

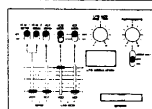


25. BENDER OFFSET

BENDER MODULE (MOD)



JUPITER-8



See appendices for adjustment locations and glossary.

1. Connect scope to TP-4 of (Upper - MOD A; Lower - MOD E) with A-442 reference to H IN.

2. Press A2 key, adjust MASTER TUNE for stationary Lissajous.

3. Set VCO MOD switch to on, adjust VR1 (Upper) or VR2 (Lower) for stationary Lissajous.

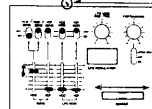
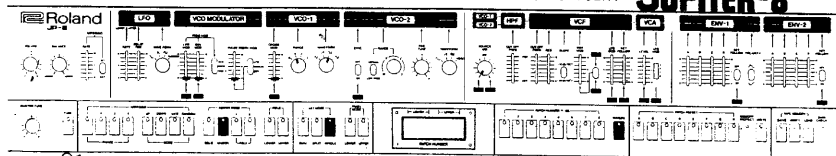
NOTE: On JP-8 S/N **0700—, next comes para. 25-1, BENDER LEVEL.

25-1. BENDER LEVEL

BENDER MODULE (MOD)

APPLICABLE S/N with **0700 and SUBSEQUENT

JUPITER-8



VR3 BENDER ADJ

1. Connect scope to TP-4 of any MOD. Press A2 key, adjust timebase and vernier (VARI) to display one complete cycle.

2. Press A3 key. Sway and hold BENDER Lever at extreme left, adjust VCO BEND to display 1 cycle.

3. Press A1 key. Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.

26. FSK

CPU

See appendices for glossary.

1. Join TAPE MEMORY LOAD and DUMP jacks via cable.

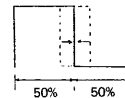
NOTE: DUMP is renamed as SAVE on later products.

2. Connect scope to CPU TP-7.

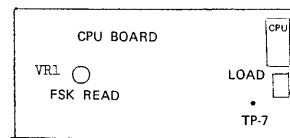
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as -| -| -| -|.

4. Set CPU VR1 for 50% duty cycle.

5. Push VERIFY again at the end of adjustment.

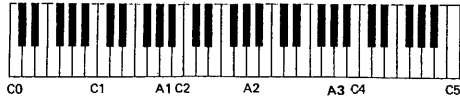


1:1

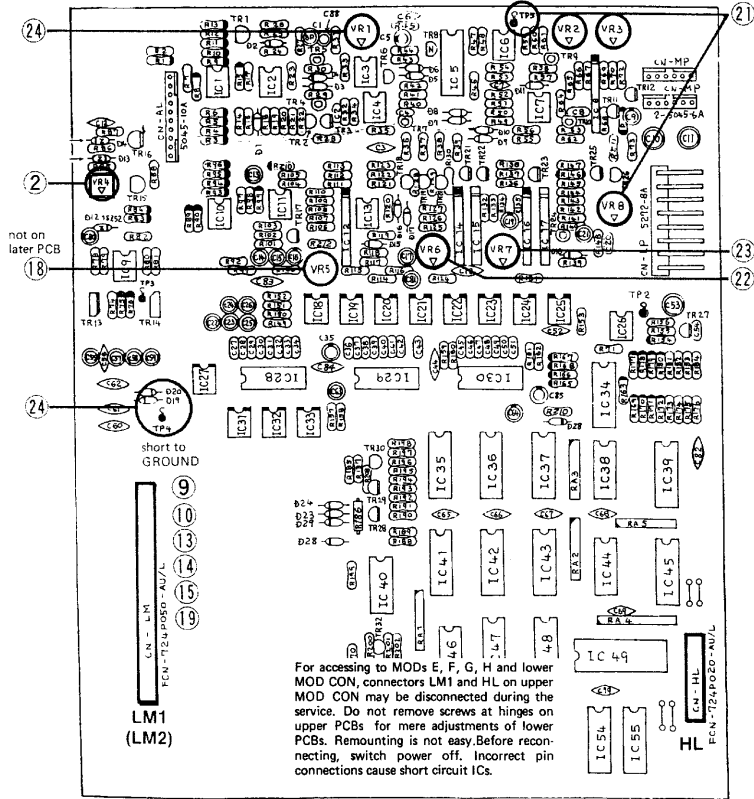


APPENDIX I

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS



MODULE CONTROLLER BOARD

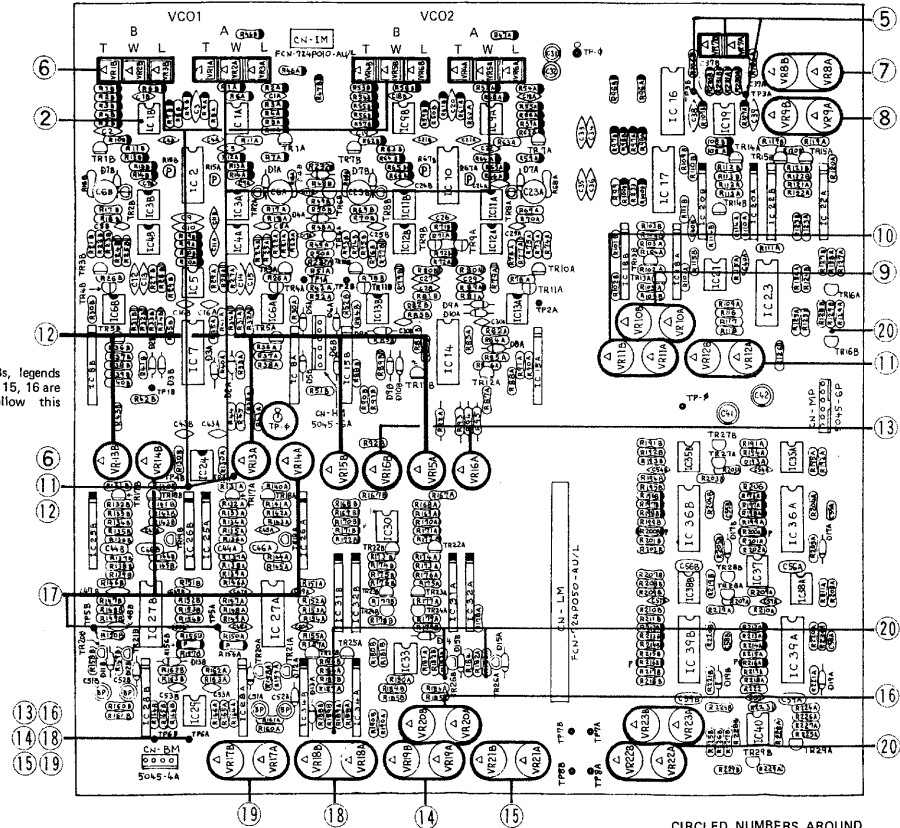


APPENDIX II MODULE BOARD

GLOSSARY

DVM	Digital Voltmeter
SCOPE	Oscilloscope
CPU	CPU Board
MOD	Module Board Module (VOICE)
CON	Module Controller Board
INT	Interface Board

On early PCBs, legends for VR13, 14, 15, 16 are incorrect. Follow this arrangement.



JP-8 SERVICE NOTES

PART 2

The following pages cover the information of Engineering changes and various aspects of JP-8 affected by the changes.

DESIGNE CHANGES THAT CHANGE FEATURE OF THE JP-8

DAC

To have JP-8 more stable in pitch, DAC for KCVs is changed from 12-bit to 14-bit version.

KEY SPLIT POINT

To make JP-8 more convenient for the user to play on, key split point becomes under the control of the player.

DIGITAL COMMUNICATION INTERFACE OC-8 & DCB

To have JP-8 externally controlled through Digital Data Bus connecting either to digitally operating "musical instrument" or to Analog/Digital Interface Unit (e.g. OP-8 that accepts analog CVs in parallel), Digital Communication Interface Board (DCIB) is built in.

OC-8: First, DCIB is named OC-8 and sold as an optional kit.

DCB: Second, another version of DCIB, called DCB is incorporated in the later JP-8 as a standard feature.

The above-mentioned changes and other significant changes not found on the First Edition of JP-8 Service Notes are listed on the table right.

PARTS LIST CHANGE

SEE P. 47

APPENDIX

SEE PP. 48~50

PCB LAYOUTS FOR EARLY 500 JP-8's MODULE BOARD MODULE CONTROLLER BOARD

Not published previously, these drawings will help to trace signal paths on old PCBs.

CHANGE INFORMATION

EFFECTIVE SERIAL NUMBER	MAJOR CHANGE	PART INVOLVED	REMARKS
Below 171700	OC-8 (OPTION): TEST PRODUCTION built into JP-8 with programmable KEY SPLIT feature	PROM Program (CUP board): IC34—IC36 Version from 1.0 to 2.1	made only on a few JP-8's see table on the next page
171700 181899	D/A CONVERTER . . . from 12-bit to 14-bit format	INTERFACE BOARD: PCB 052H268 to 052H268 DAC (IC14) from Am6012 to ITS80141 Some ICs and circuits CPU BOARD: PROM programs (IC34—IC36) Version 1.0 to 3.1	14-bit INTERFACE BOARD is compatible with the 12-bit pcb only when PROMs of CPU BOARD are replaced with of version 3.1 or 3.2 see P. 34 for detail
	OC-8 (OPTION): made as a commercially available kit for both 12- and 14-bit versions	ROMs IC34—IC36 of CPU BOARD to be replaced upon installing OC-8	IC34—IC36 must be 3.2 version and are supplied in an OC-8 kit together with PROM IC33 containing communi- cation program
181900	PROMs PROGRAM . . . revised to be compatible with those stored in OC-8 kit PROMs	CPU BOARD: IC34—IC36 from 3.1 to 3.2 version	additional PROM 3.4D (IC33) only is necessary upon installing OC-8 see table on the next page for detail
202100	MODULATION CIRCUITS: To have U and L sounds kept balanced	MODULE CONTROLLER BOARD: PCB from 052H269 to 052H269 some circuits	when U or L board is replaced with new one, the remainder should be slightly modified. see pp. 36—38 for detail
202210	RAM (MODULE CONTROLLER BOARD IC 49): make equivalent RAM usable	CPU BOARD: IC23	short pin 5 of IC23 to ground see p. 38 for modification
242750	LED DISPLAY: adopt brighter LED	PANEL BOARD F: from LN526RA to LN5620A	new and old LEDs are different in color and brightness mix use should be avoided for uniformity
272850	FUNCTION SWITCH: LED to diffusive, brighter type	PANEL BOARD E: PANEL BOARD G: function switch from KHC11901 to KHC11026 (LED from AR3432S to SEL2210R)	
282880	DCB BOARD (similar to OC-8): built into JP-8 as a standard feature	CPU BOARD MODULE CONTROLLER BOARD PANEL BOARD A	drawings related to this change begin at p. 40

HOW TO IDENTIFY PROM VERSION

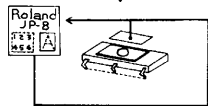
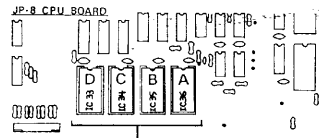
CPU BOARD

Version is indicated by hand written number or marking on the label as shown below. Version can be displayed in PATCH NUMBER window (LOWER). Turn the JP-8 on while pressing PATCH NUMBER buttons 1 and 3.

NOTES:

In 0.7 or 1.0 version, displayed number will change quickly from 07 (10) to 13.

In 3.2 (A, B, C) and 3.3D (3.4) arrangement, number 33 (34) will change to 32 if PROM D is removed.



PROM VERSION PROGRAM

0.7 1.0	12-BIT DAC FIXED KEY SPLIT POINT
2.0	12-BIT DAC VARIABLE KEY SPLIT POINT
2.1D	DIGITAL COMMUNICATION INTERFACE
3.1	14-BIT DAC VARIABLE KEY SPLIT POINT
3.2 2)	14-BIT DAC VARIABLE KEY SPLIT POINT
3.3D (3.4D)	DIGITAL COMMUNICATION INTERFACE

- 1) This is a special version. Replace each with the same one, or replace all four with a set of 3.2 and 3.4D version.
- 2) Co-operates with 3.3D or 3.4D for Digital Communication Interface.

When need arises to modify the JP-8 or to replace parts:

First consult the table below, then refer to the right as necessary.

PROM REPLACEMENT

When replacing PROMs A, B and C with different version, replace them in a set.

Version 3.2 can replace 3.1, 1.0 and 0.7

Version 3.1 can replace 1.0 and 0.7

The reverse does not hold true.

ROM 3.4 can replace 3.3D and vice versa.

NOTES:

PROM D is required only when OC-8 or DCB BOARD is present.

PROM D must be used together with A, B, C of 3.2 version and up.

PROM D contains diagnostic programs.

Refer to P.46 for test procedure.

Difference between 3.3D and 3.4D is that the latter has debugged diagnostic program.

INTERFACE BOARD	p. 34
MODULE CONTROLLER BOARD	pp. 37, 38
RAM IC49 of MOD CON BOARD	p. 38
CPU BOARD (in relation to RAM IC 49)	p. 38
OC-8	OP-8 (OC-8) Service Notes

When new feature is required, replace existing part(s) with the one indicated by ●.

SERIAL NUMBER	PROM VERSION				DISPLAY	The JP-8 may be or may have	Features of the JP-8	Addable new feature	PROM	VERSION	INTERFACE BOARD w/14-bit DAC	by-product
	A	B	C	D					A, B, C 3.2	D 3.3 or 3.4		
PROTOTYPE	0.7				07	as produced	DAC 12-bit KEY SPLIT POINT Fix	DA 14-bit SPLIT POINT Variable	●	/	●	Variable Split point
030100	1.0				10	as produced	OC-8 less	OC-8 built in	●	●	/	Variable Split point
	JP-8 2.1D				21	OC-8: installed at the factory	DAC 12-bit KEY SPLIT POINT Variable	DA 14-bit	●	●	●	/
171699	(3.2)				33 or 34	OC-8: built in as option	OC-8 built in	/	●	/	●	/
171700	3.2				31	as produced	DA 14-bit	/	●	●	/	/
181899	3.2				32	as produced	KEY SPLIT POINT Variable OC-8 less	OC-8 built in	/	●	/	/
181900	3.2				32	as produced	OC-8 less	/	/	●	/	/
282879	3.2				32	as produced	OC-8 less	/	/	●	/	/
171700-272829	(3.2)				34	OC-8: built in as option	DA 14-bit KEY SPLIT POINT Variable	/	/	/	/	/
2828800	(3.2)				34	DCB: built in as a standard feature	OC-8 (DCB) built in	/	/	/	/	/

INTERFACE BOARD OPH122A

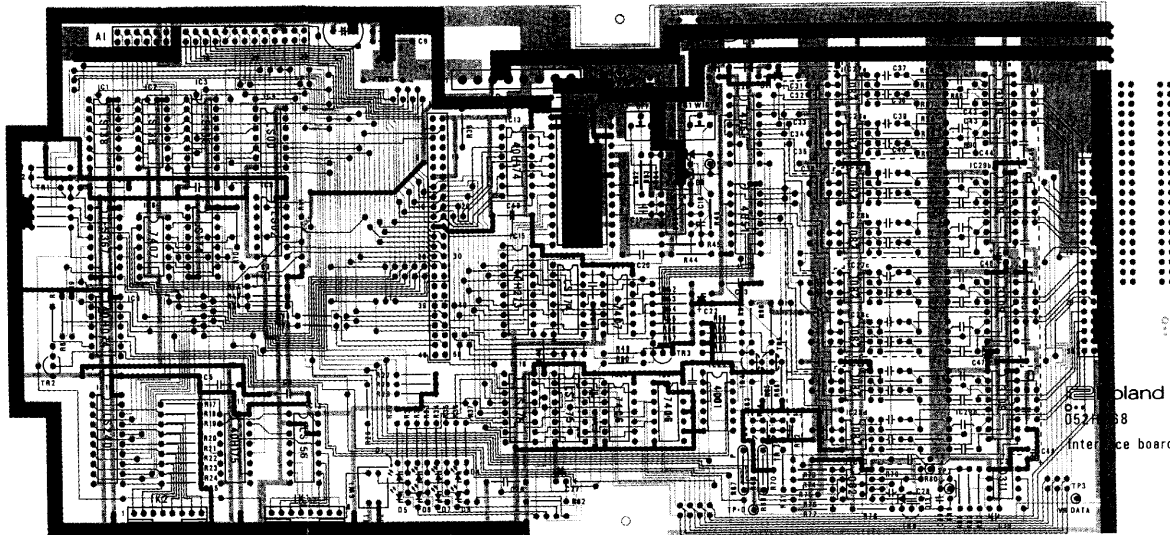
(149H122A) (pcb 052H268)

SN 171700 and higher

MAJOR CHANGES

D/A CONVERTER 14BIT

KEY SPLIT POINT PROGRAMMABLE



This board can replace 12-bit INTERFACE BOARD when PROMs of CPU board are of correct version. See right below.

Besides suffix (A, B, etc.), the PCBs occasionally bear marks "●" and/or "○" above its code number to show the edition.

● stands for 1, and ○ for 5.

Example: ○*** = 8th edition

The D/A Converter IC14 is changed from 12-bit Am6012 to 14-bit ITS80141 with this PCB version. Along with the change the following parts are also changed.

PART	From	To
Latch	LS273 (TTL, IC13)	40H273 (CMOS, IC15)
	LS175 (TTL, IC15)	40H174 (CMOS, IC13)
Multiplexer	LS175 (TTL, IC11)	40H175 (CMOS)
	4051 (IC25, IC26)	HD14051 (Hitachi only)
Flip-flop	74LS74 (IC9)	TC4013
		(SN212330-UP TC40H74)
Gate	LS02 (IC22)	TC4001

Prepare PROMs for CPU board:

A, B, C

3.1 version

or

3.2 version (inevitable when OC-8 exists)
for IC34-IC36

D (when OC-8 is built in)

3.3 or 3.4 version for IC33

Replace existing PROMs with these PROMs.

Adjust DAC circuit, referring to "4. DAC" on p.25 of this book.

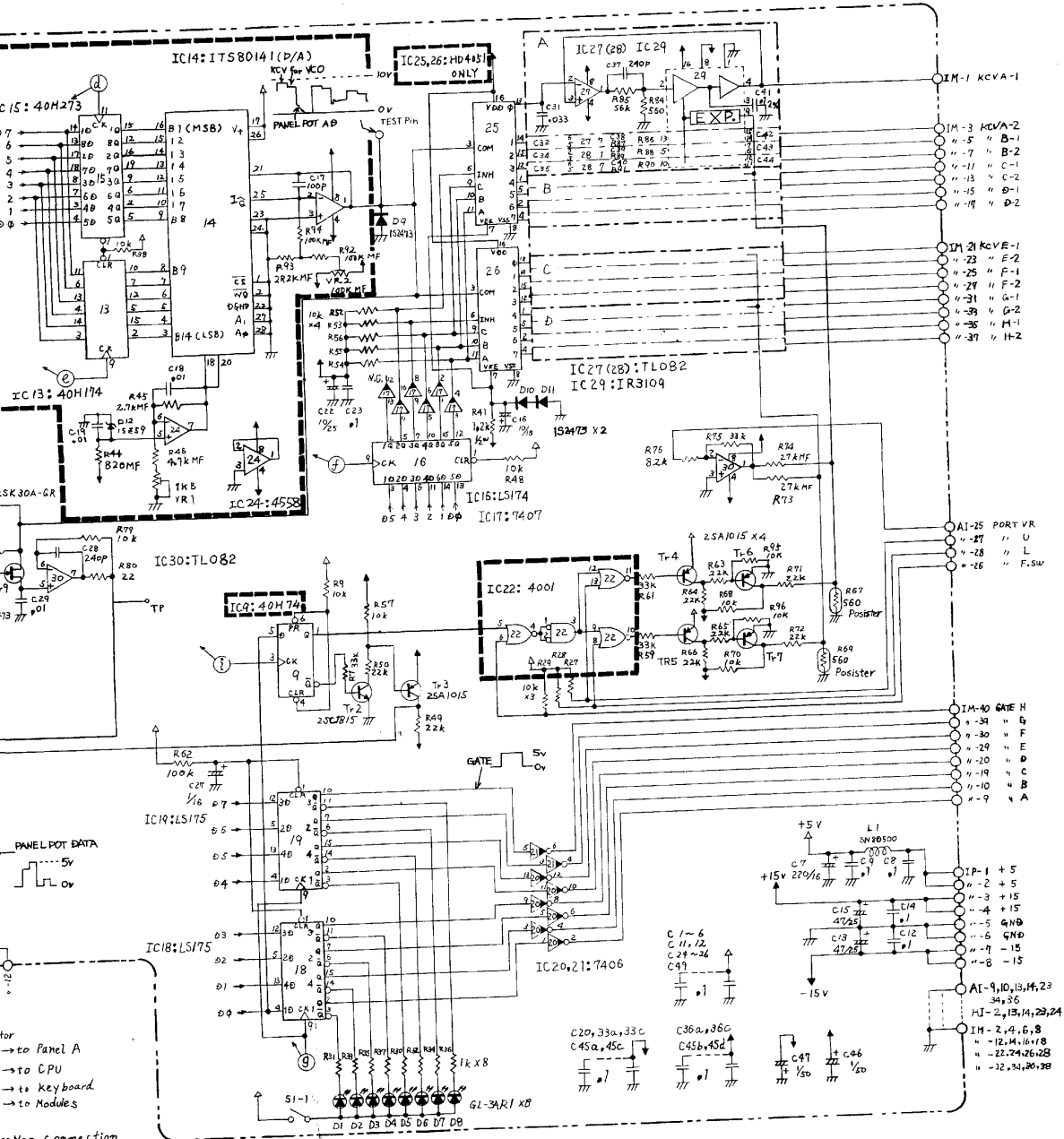
SUBSTITUTING THIS BOARD FOR 12-BIT DAC BOARD

NOTES:

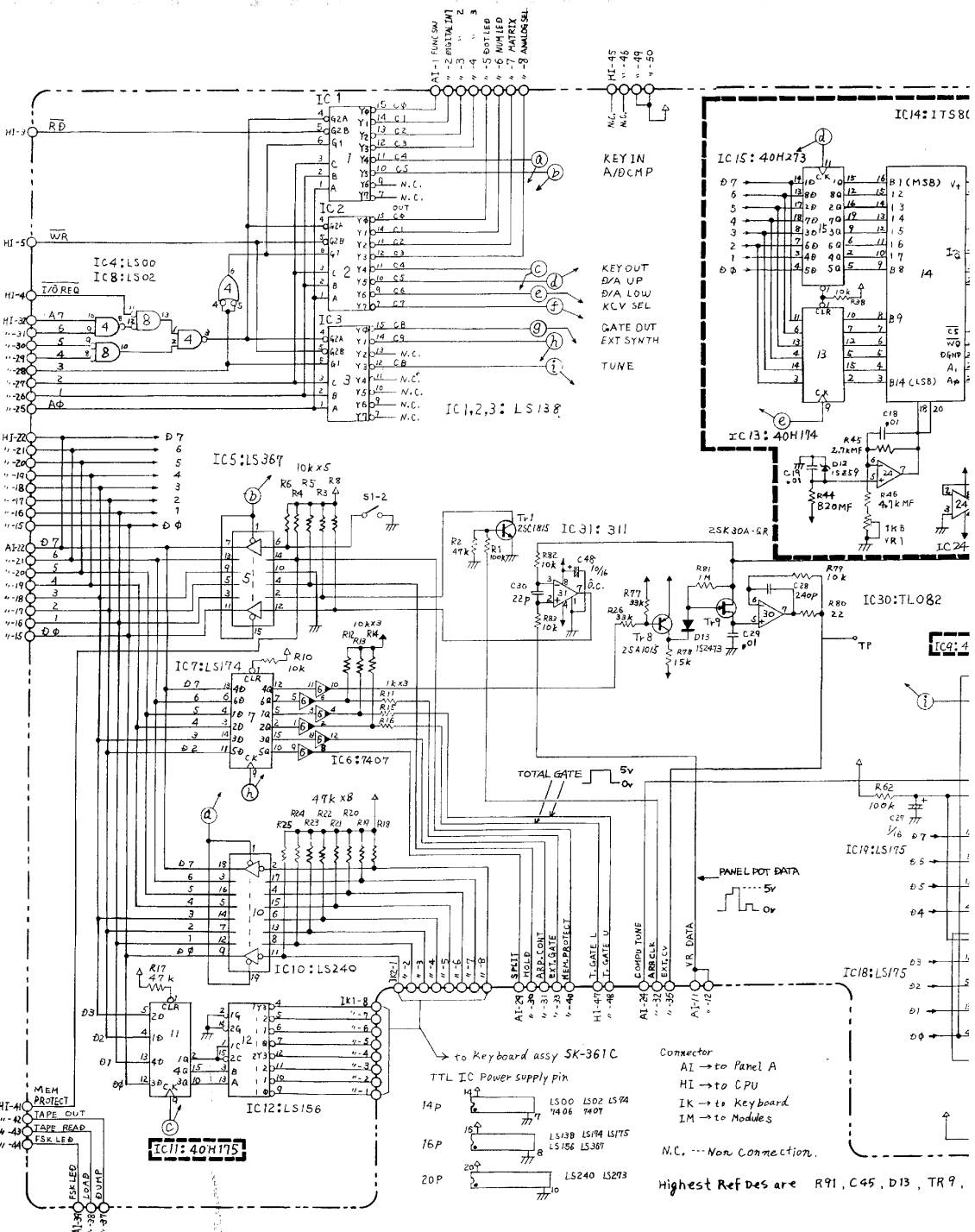
This interchange does not affect adjustment procedures except that the letter "PLL" are displayed in PATCH NUMBER window after -1-1-1 during FSK adjustment steps.

At the end of Computune cycle(s), defective VCO that has not "tuned-in" is indicated in MANUAL and PATCH NUMBER or PRESET buttons.

See p.39 for indicators and difference in computuning between 12-bit and 14-bit systems.



... Non Connection.
 st Ref Des are R91, C45, D13, TR9, IC31, VR2, L1, SW1



to keyboard assy SK-361C

TTL IC Power supply pin

14p L500 L502 L504
1406 7407

16p L513B L519A L5175
L5156 L5387

20p L5240 L5273

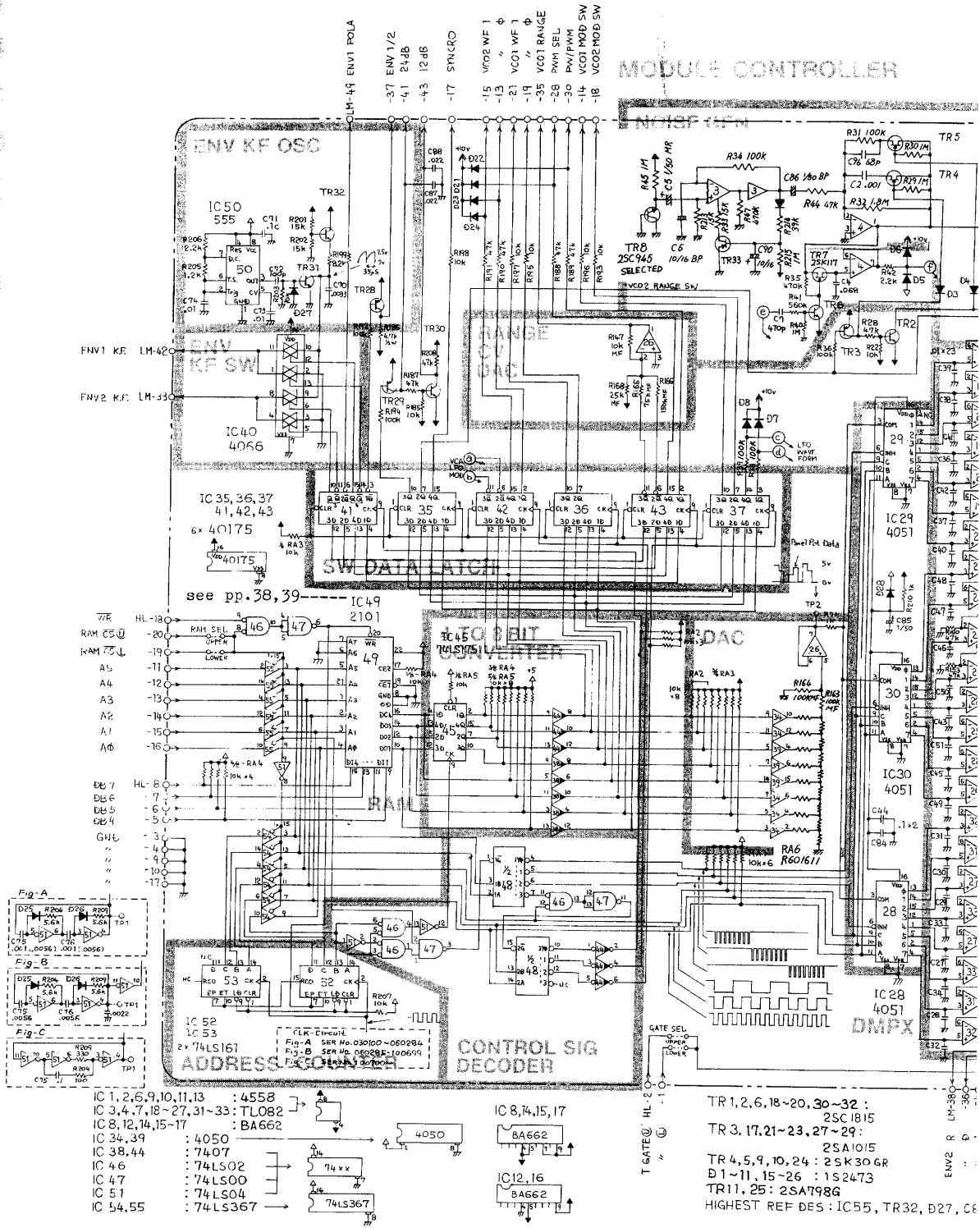
Connector

AI → to Panel A
HI → to CPU
IK → to keyboard
IM → to Modules

N.C. --- Non Connection.

Highest Ref Des are R91, C45, D13, TR 9.

MODULE CONTROLLER

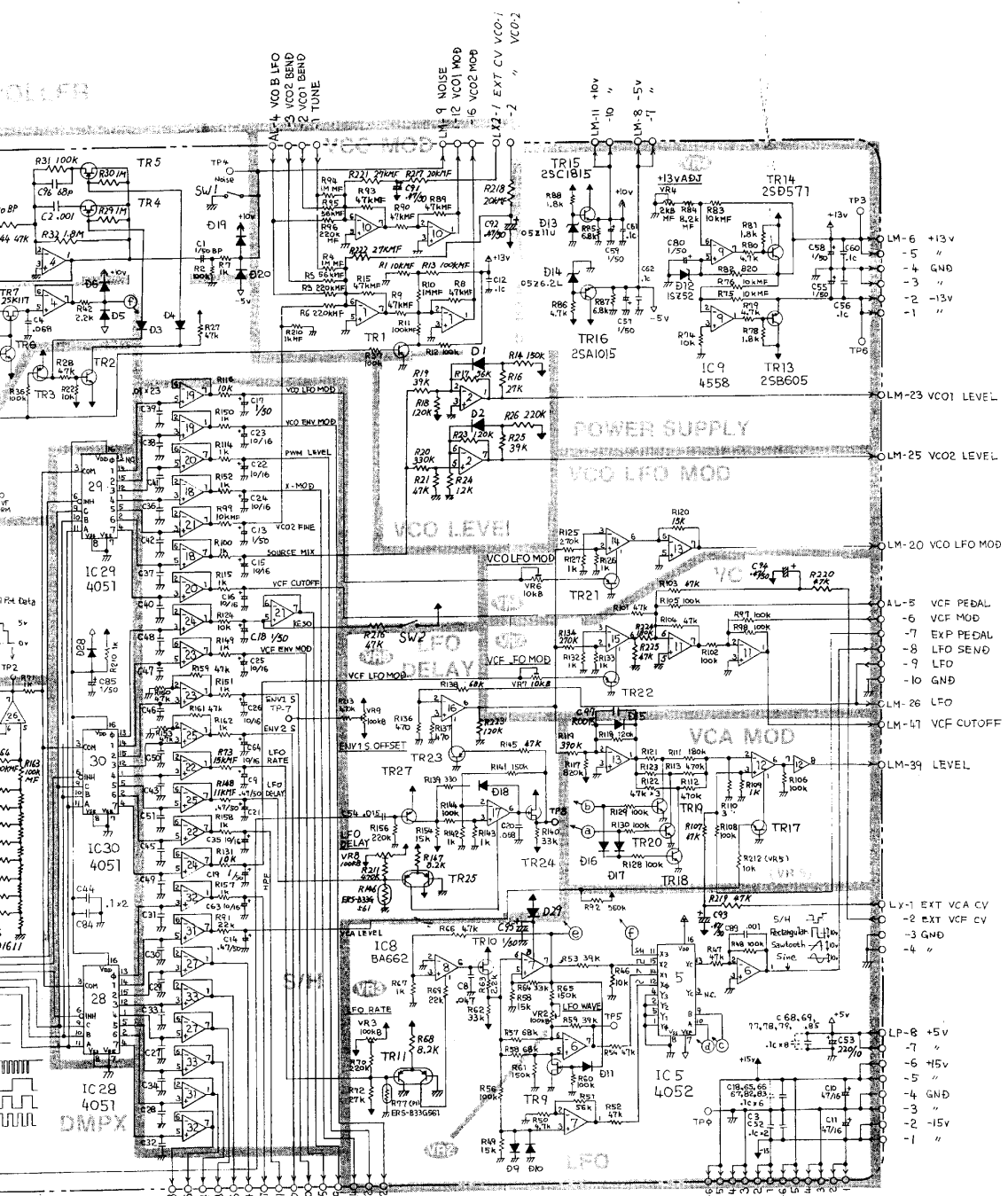


- IC 1, 2, 6, 9, 10, 11, 13 : 4558
- IC 3, 4, 7, 18-27, 31-33: TL082
- IC 8, 12, 14, 15-17 : BA662
- IC 34, 39 : 4050
- IC 38, 44 : 7407
- IC 46 : 74LS02
- IC 47 : 74LS00
- IC 51 : 74LS04
- IC 54, 55 : 74LS367

- IC 8, 14, 15, 17 : BA662
- IC 12, 16 : BA662

- TR 1, 2, 6, 18-20, 30-32 : 2SC1815
- TR 3, 17, 21-23, 27-29 : 2SA1015
- TR 4, 5, 9, 10, 24 : 2SK306R
- D 1-11, 15-26 : 1S2473
- TR 11, 25 : 2SA798G
- HIGHEST REF DES: IC55, TR32, D27, C6

01:FR



- LM-30 ~ 32 : 25C1815
- LM-29 : 25A1015
- LM-24 : 25K30GR
- LM-6 : 152473
- LM-1 : SA798G
- DES : IC55, TR32, D27, C88, R212, RA5, VR9

GUIDES ON REPLACEMENT

MODULE CONTROLLER BOARD

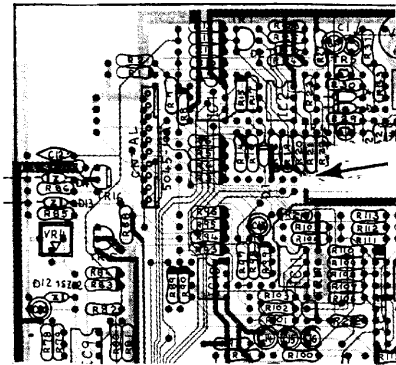
(For early 500 units, see p.48)

When replacing OPH123 with OPH123A, be sure to proceed the following.

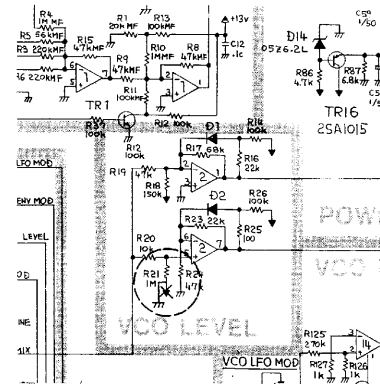
Check IC49 on the both PCBs (being replaced and replacement) for name. If 2101 is on the existing PCB and 5101 on the replacement, take the modification illustrated below.

When replacing Upper board or Lower only:

Adjust VR1 (NOISE LEVEL) of unchanged MOD CON board to match the noise level of new board which omits the adjustment. Reconnect R21 of unchanged MOD CON, referring to drawing to the right. This will eliminate possible loudness differences between U and L voices.



Disconnect R21 lead at negative end and solder it to the nearest ground foil.



IC49 OF MOD CON BOARD (MODIFICATION ON CPU BOARD)

(RAMs 2101 and 5101)

Below, two minor modifications (independent of RAM change) are also indicated:

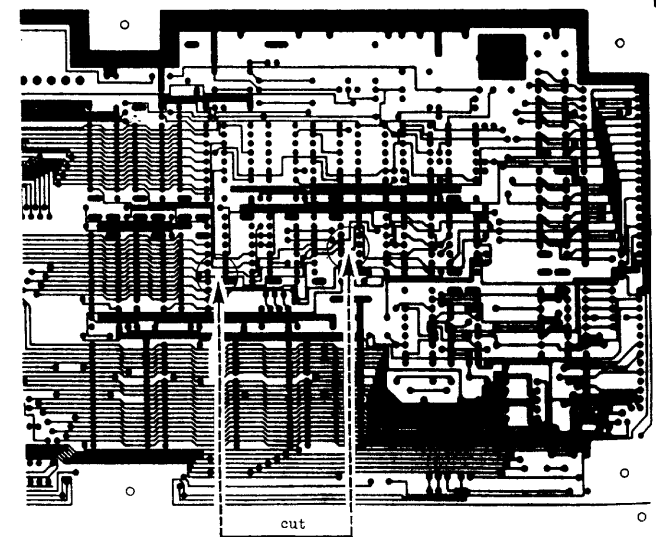
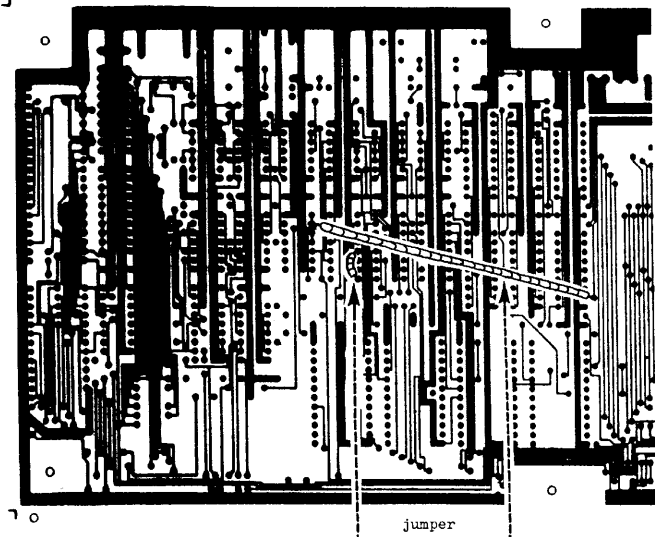
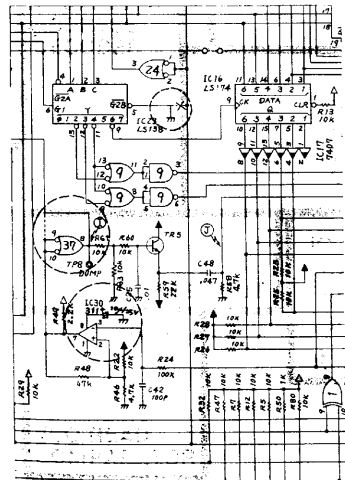
Reconnection of IC37 and addition of 10UF at IC30 pin 8

Insertion of 5101 into a place previously occupied by 2101 requires pin 5 of IC23 on CPU board to be grounded. This reconnection as illustrated is to protect the data on panel control from garbled — while a control is being reset, some of other controls

are also detected as moving; in extreme case no voice would sound. This is due to the fact that two RAMs differently respond to the same timing signal.

This modification has no adverse effect on 2101.

Factory modification SN 202210-UP

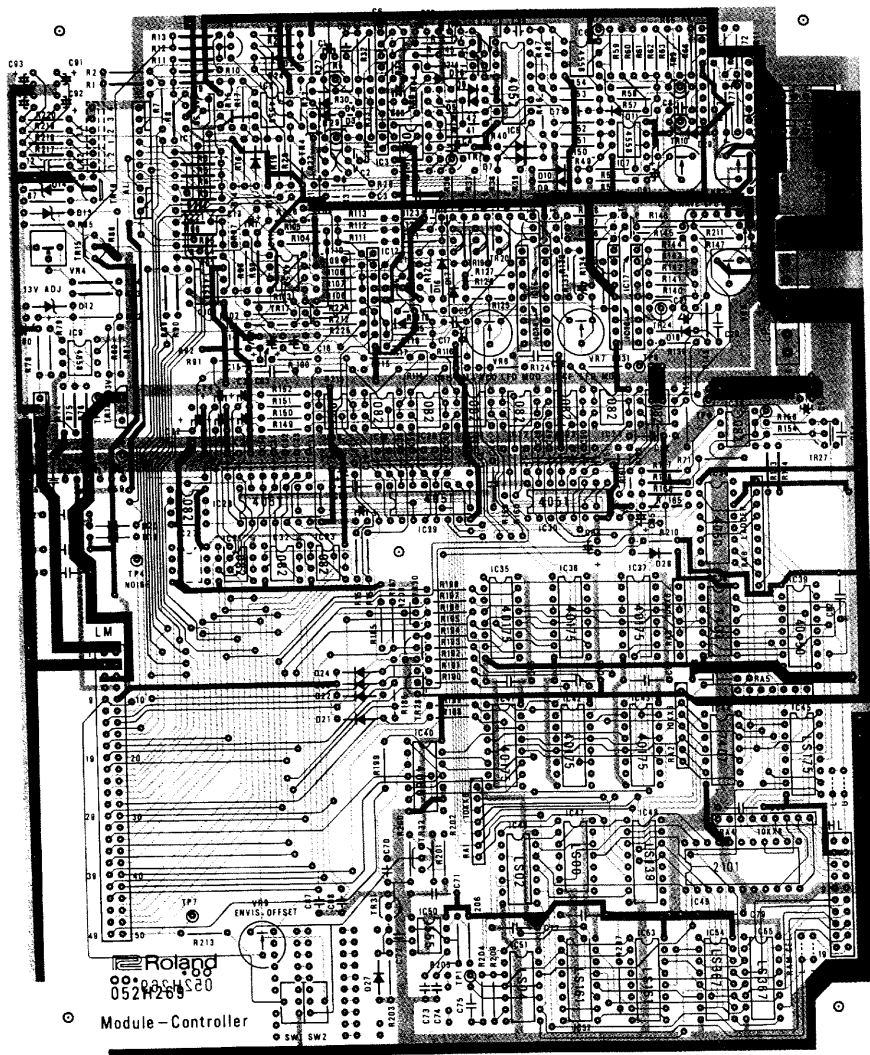


MODULE CONTROLLER BOARD SN 202100 and UP
OPH123A (149H123A) (pcb 052H269)

IMPORTANT
 When replacing MOD CON BOARD or RAM IC49,
SEE PAGE 38 (P.48 for early 500 units).

CHANGE INFORMATION

(Each heading is followed by address to the circuit diagram.)



1. NOISE GENERATOR (D-H, 18-27)

IC3: from TL082 to BA662 having AGC.
 NOISE LEVEL VR1: omitted

SAMPLING SIGNAL

Previous circuit:

Only white noise is routed to S/H circuit regardless of VCO-2 RANGE position.

New circuit:

Pink noise is selected for S/H when RANGE is in LOW position.

2. D/A CONVERTER (O-R, 23)

Ladder Resistors: from discrete to resistor array

3. NOISE KILLER SWITCH (D-E, 28)

Newly attached for cutting off noise signals. Used in particular adjustments. Close this switch when step states "Place a ground to MOD CON TP-4".

4. RESONANCE SWITCH (M,33)

To emphasis regeneration to the point of oscillation. Used for factory adjustment only.

5. LFO DELAY CONTROL (R, 33)

From TR25 and TR26 to single paired-transistor TR25 to have U and L delay times synchronize with each other.

6. LFO RATE (V,33)

From TR11 and TR12 to single paired-transistor TR11. To minimize speed difference between U and L LFOs.

7. Add D29 and C95 to +B pin of IC7 (S, 36) to stabilize the supply voltage

8. Add RC filters on EXT CV lines (L, 43; S, 41; E, 35; D, 33)

To filter out noise induced into EXT CV.

9. VCO LEVEL (J, 33-34)

Apply a ground to pin 5 of IC2 through R21, previously -15V. Change resistors values in this section

To set VCO-1 and VCO-2 audio levels to an equal amount when SOURCE MIX is set at 12 o'clock position.

To have the same volume changes in VCO-1 and VCO-2 sounds, that is, the change in volume of VCO-1 when SOURCE MIX is being rotated toward VCO-1 is the same as that of VCO-2 when S.M. being toward VCO2.

10. VCA MOD (O, 38-39)

Add C97 across pins 1 and 2 of IC13

To eliminate click noises at positive or negative going transient.

11. Add TP-8 (Q, 36-37)

For factory adjustment only.

IC49, RAM 2101 and 5101 SN 202210-UP

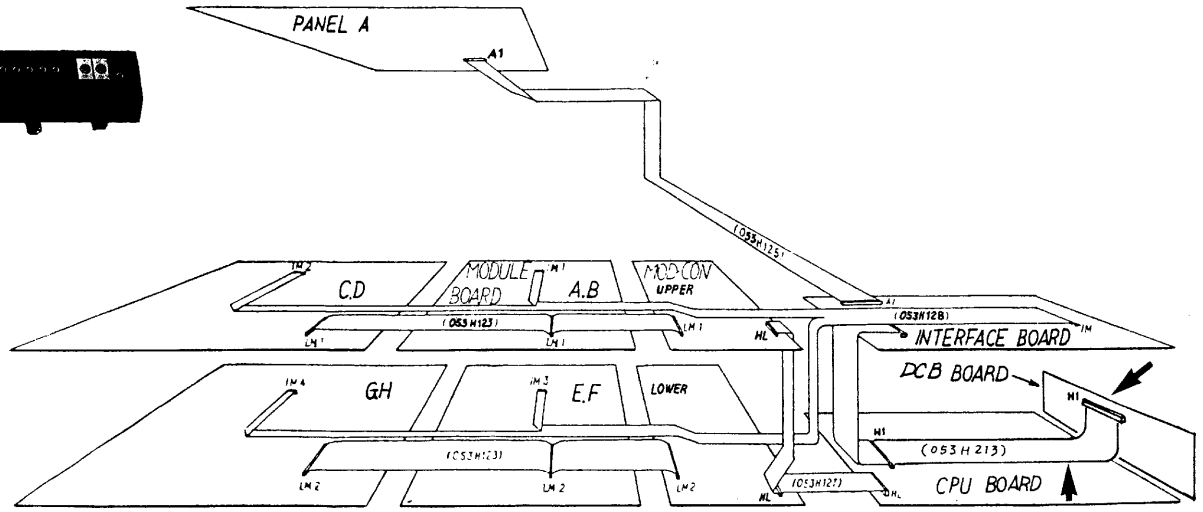
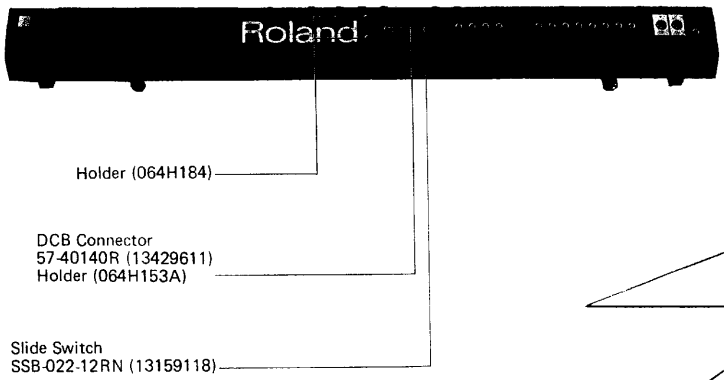
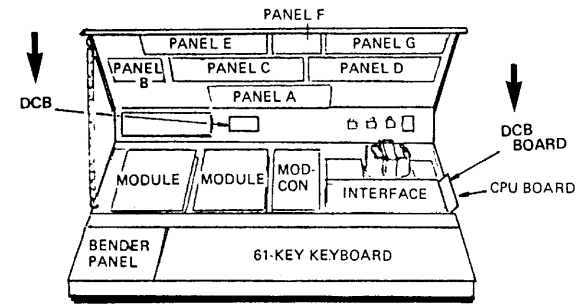
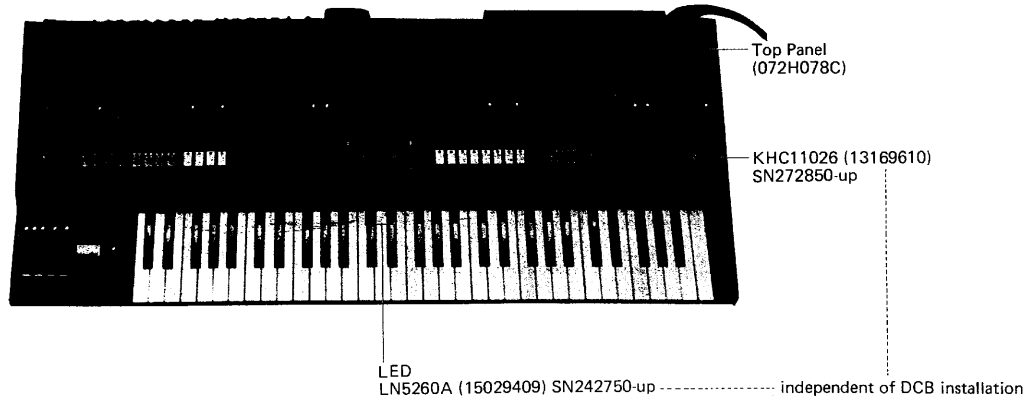
Often, RAM 2101 is substituted by 5101 upon manufacturing or shipping replacement because of procurement problem.

RAMs of these models have different characteristics in timing response.

To make both RAMs compatible, factory modification on CPU board started with above Serial number. (See p.38 for detail.)

NOTE:
 Beside suffix (A, B, etc.), the PCBs occasionally bear marks "w" and/or "o" above its code number to show the edition. "s" stands for 1, and "o" for 5. example: o... 8th edition.

CHANGES, MODIFICATIONS, ADDITIONS INVOLVED IN IMPLEMENTING DCB (Digital Communication Bus) BOARD pp.40-47



CIRCUIT DESCRIPTION

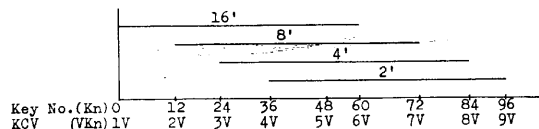
This circuit description applies to the JP-8 with serial numbers 171700 and up where DAC changed from 12- to 14-bit version, and concentrates on computune program which is revised in line with the change.

This description makes reference to pages 6 and 7 "WIDTH" and "KCV" of the Circuit Description of First Edition issued separately.

WIDTH

P. 6 Change title to WIDTH & TUNE

The coverage of the JP-8 keyboard is expandable to 96 keys using footage selector (RANGE SWITCH). In the following, KCV and key designation are defined as below.



In this mutual arrangement any KCV (VKnx) at a key (Knx) is obtained from the equations:

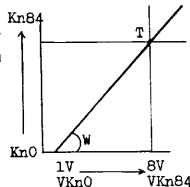
$$VKnx = VKno + W(WIDTH) \times Knx \quad (1)$$

$$\text{OR } VKnx = T(TUNE) - W(84 - Knx) \quad (2)$$

where, $W = 1/12(V)$

— voltage steps per half tone

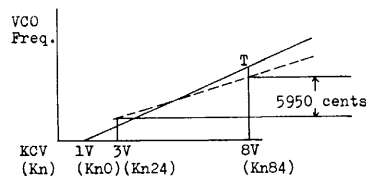
$$T = VKn84$$



In the following computuning, T is a reference voltage in calculating every KCVs to the equation (2) above.

Upon power on for the JP-8, computune program starts frequency measurements at two points with MOD.A VCO-1 by applying KCV of Kn24(3V) and VKn84(8V) to it. If the VCO output is 20 cents higher than expected pitch at 3V KCV, and 30 cents lower at 8V as shown in the figure right, the factor W is given by:

$$\frac{8 - 3(V)}{9570 - 3620(\text{cent})} = 0.084$$



Substituting 0.084 for W in equation (2) above would provide the VCO with KCVs for every keys, and the VCO will oscillate in 1V/oct steps with most of pitches slightly out of tune.

To bring each note in tune, the program first adds fine tune voltage (bias) ... $0.084 \times \frac{30}{100}(\text{cent}) = 0.0252V$ — to T. Then, finds KCVs for every notes by applying equation (2).

$$\text{Example: } VKn24 = 8.025(T) - 0.084(W) \times (84 - 24) = 2.985V.$$

When compare this WIDTH with the WIDTH determined by previous 12-bit system, the new system provides more precise resultant because of wider measurement range.

INITIAL TUNING UPON POWER ON

When the power is first turned on for the JP-8, thermally unstable VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that computune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program ceases measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program resumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time.

Most VCOs outside tolerances after completion of the second execution might be brought closer and closer to desired pitches if the computune program is forced to repeat the operation by manual triggering of TUNE button. (See next paragraph.)

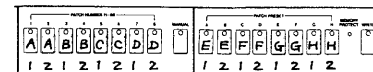
Tuning sequence is visually confirmed on flashing LEDs in the PATCH buttons.

VCO BEING MEASURED

PATCH NO.	1st cycle		2nd cycle	
	MODULE	VCO	MODULE	VCO
1	A	1	E	1
2	A	2	E	2
3	B	1	F	1
.
.
.
8	D	2	H	2

However, when one PATCH LED stays on while MANUAL LED is flashing, they are indicating failure in that VCO. The computune program cannot correct such a VCO as is indicated by a PATCH button as below, and does not proceed to the next VCO unless one of function switches is touched.

MODULE
VCO



COMPUTUNE WITH TUNE BUTTON

When the computune program is triggered manually with TUNE button (after power-on-tune), it runs only once for each VCO since the program already had data on fine tune, and drastical change in VCO frequencies is likely to occur. If the program fails to compensate frequency drift, iterative tapping of "TUNE" will bring VCO closer to correct pitch. Relying on this method is preferable only in an emergency; the cause of out of tune must be eliminated as early as possible.

KCV (INTERFACE BOARD)

P.7 Lines 9 and 10: Delete

Lines 11-17: Reads as follows.

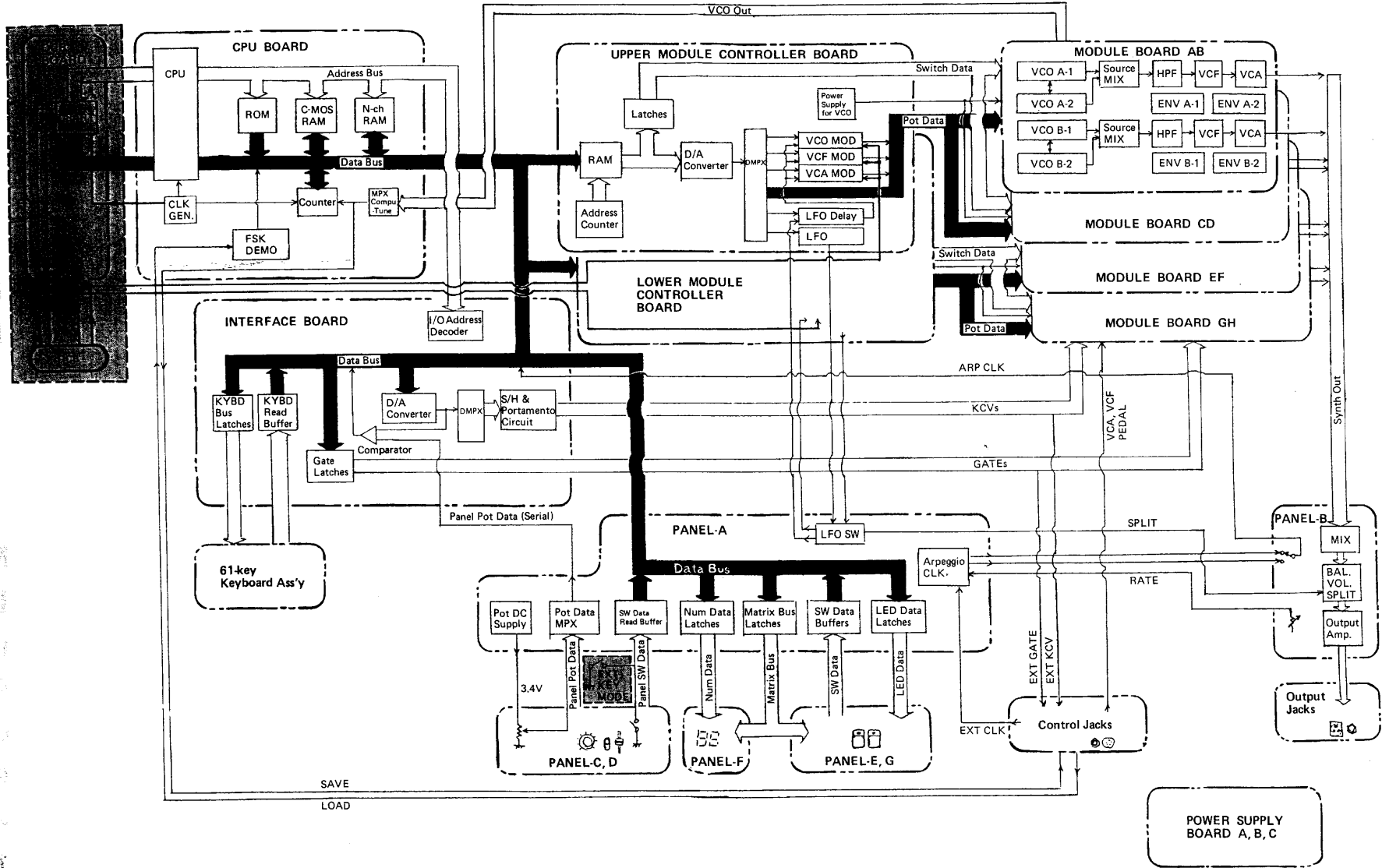
Each KCV data is represented in 14-bit format and is divided into two pieces—MS (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is $10V \div 2^{14}(\text{bit}) = 0.6mV$, nearly equals 0.7 cents in pitch. Durig I/V conversion in $\frac{1}{2}IC24$, CV for EXT. jack is scaled 1V/oct.

CORPECTION

CIRCUIT DESCRIPTION

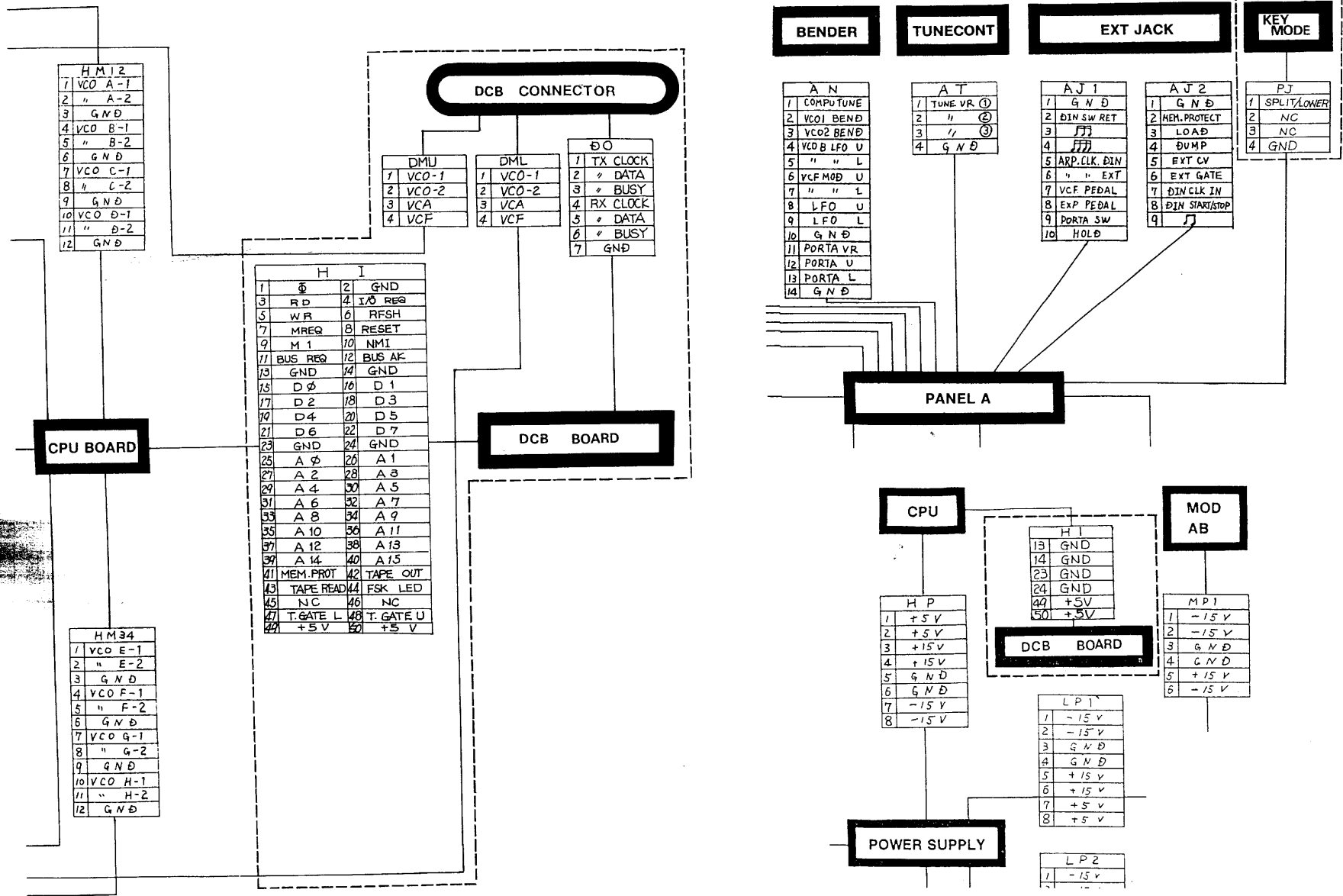
P. 11: PUSH SWITCH SCANNING

Push switches (function switches with LED) are read every approximately 25ms (not 1ms). See timing chart on page 3 of the Circuit Description. LEDs are lit every 1ms when INT signal is applied from IC26 which in turn is timed by the signal generated at pin 17 of IC40. Failure of INT signal causes no LED driving signal, but has no relation to the switch reading performance.



SAVE
LOAD

POWER SUPPLY BOARD A, B, C



HM12	
1	VCO A-1
2	" A-2
3	GND
4	VCO B-1
5	" B-2
6	GND
7	VCO C-1
8	" C-2
9	GND
10	VCO D-1
11	" D-2
12	GND

DCB CONNECTOR	

DMU	
1	VCO-1
2	VCO-2
3	VCA
4	VCF

DML	
1	VCO-1
2	VCO-2
3	VCA
4	VCF

DO	
1	TX CLOCK
2	" DATA
3	" BUSY
4	RX CLOCK
5	" DATA
6	" BUSY
7	GND

HI	
1	Φ
2	GND
3	RD
4	I/O REQ
5	WR
6	RFSH
7	MREQ
8	RESET
9	M 1
10	NMI
11	BUS REQ
12	BUS AK
13	GND
14	GND
15	D 0
16	D 1
17	D 2
18	D 3
19	D 4
20	D 5
21	D 6
22	D 7
23	GND
24	GND
25	A 0
26	A 1
27	A 2
28	A 3
29	A 4
30	A 5
31	A 6
32	A 7
33	A 8
34	A 9
35	A 10
36	A 11
37	A 12
38	A 13
39	A 14
40	A 15
41	MEM. PROT
42	TAPE OUT
43	TAPE READ
44	FSK LED
45	NC
46	NC
47	T. GATE L
48	T. GATE U
49	+5V
50	+5V

HM34	
1	VCO E-1
2	" E-2
3	GND
4	VCO F-1
5	" F-2
6	GND
7	VCO G-1
8	" G-2
9	GND
10	VCO H-1
11	" H-2
12	GND

BENDER	
--------	--

TUNECONT	
----------	--

EXT JACK	
----------	--

KEY MODE	
----------	--

AN	
1	COMPUTUNE
2	VCO1 BEND
3	VCO2 BEND
4	VCO B LFO U
5	" " L
6	VCF MOD U
7	" " L
8	LFO U
9	LFO L
10	GND
11	PORTA VR
12	PORTA U
13	PORTA L
14	GND

AT	
1	TUNE VR ①
2	" " ②
3	" " ③
4	GND

AJ1	
1	GND
2	DIN SW RET
3	FFF
4	FFF
5	ARP. CLK. DIN
6	" " EXT
7	VCF PEDAL
8	EXP PEDAL
9	PORTA SW
10	HOLD

AJ2	
1	GND
2	MEN. PROTECT
3	LOAD
4	BUMP
5	EXT CV
6	EXT GATE
7	DIN CLK IN
8	DIN START/STOP
9	J

PJ	
1	SPLIT/LOWER
2	NC
3	NC
4	GND

PANEL A	
---------	--

CPU	
-----	--

MOD AB	
--------	--

HI	
13	GND
14	GND
23	GND
24	GND
49	+5V
50	+5V

HP	
1	+5V
2	+5V
3	+15V
4	+15V
5	GND
6	GND
7	-15V
8	-15V

LP1	
1	-15V
2	-15V
3	GND
4	GND
5	+15V
6	+15V
7	+5V
8	+5V

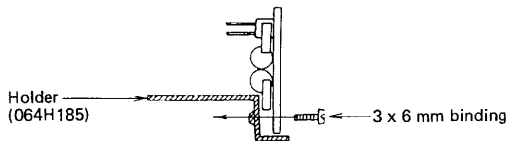
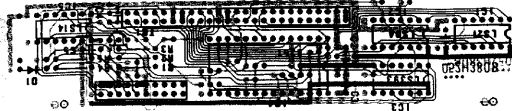
POWER SUPPLY	
--------------	--

LP2	
1	-15V

DCB BOARD

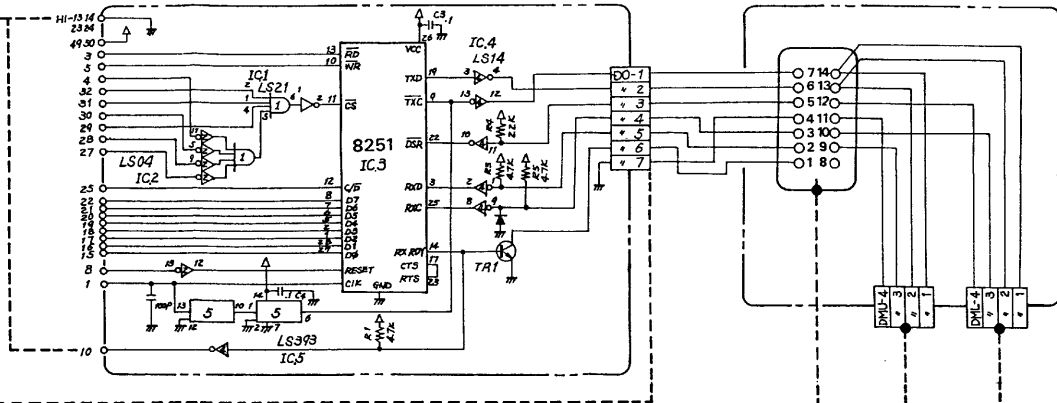
OPH220 (149H220) (pcb 052H380B)

FCN724PC50-AU/L



5045-07A
DD

DCB BOARD

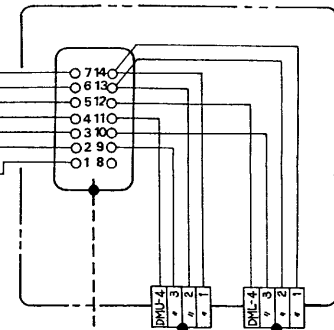


DCB PIN ASSIGNMENT

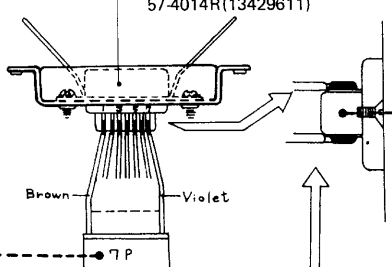
PIN	DESCRIPTION	PIN	DESCRIPTION
1	RX BUSY	8	NC
2	* DATA	9	VCA UPPER
3	* CLOCK	10	VCF LOWER
4	GND	11	VCF UPPER
6	* DATA	12	VCO-2
7	* CLOCK	14	VCO-1

DCB (Digital Communication Bus)

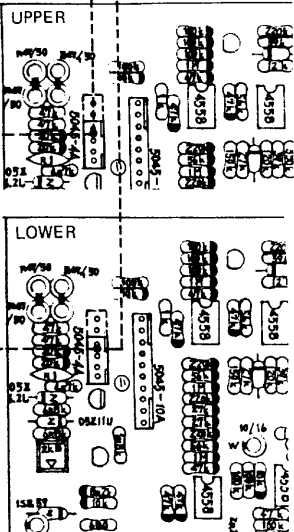
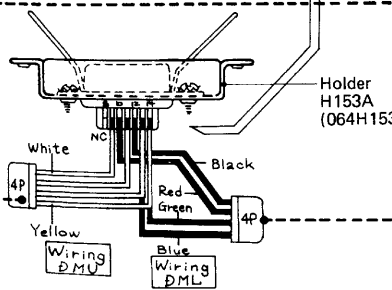
DCB CONNECTOR ASS'Y



Connector 57-4014R (13429611)

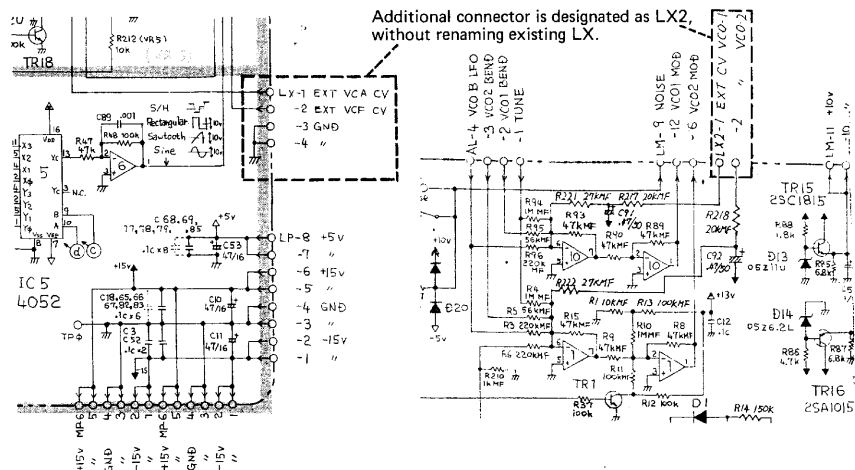


Holder H153A (064H153A)

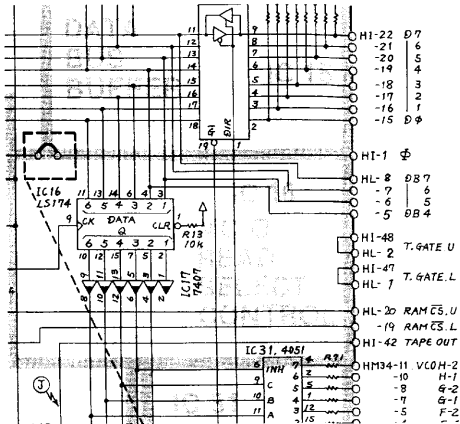
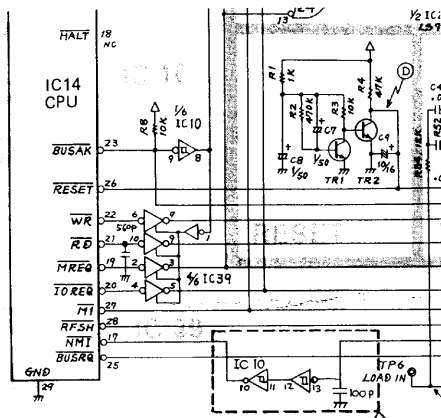


MODULE CONTROLLER BOARD

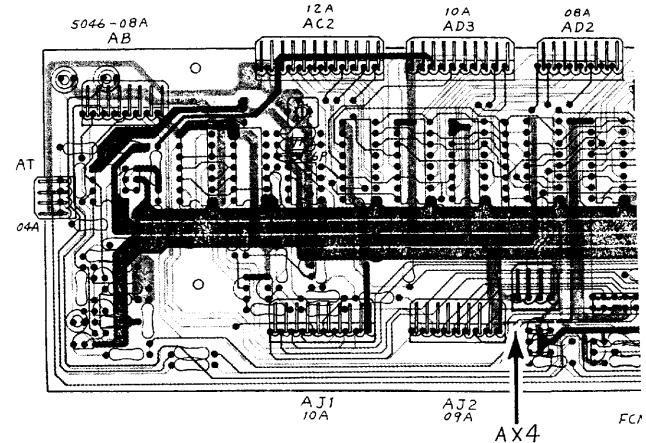
Additional connector is designated as LX2, without renaming existing LX.



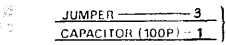
Circuits Changes related to DCB Board Installation



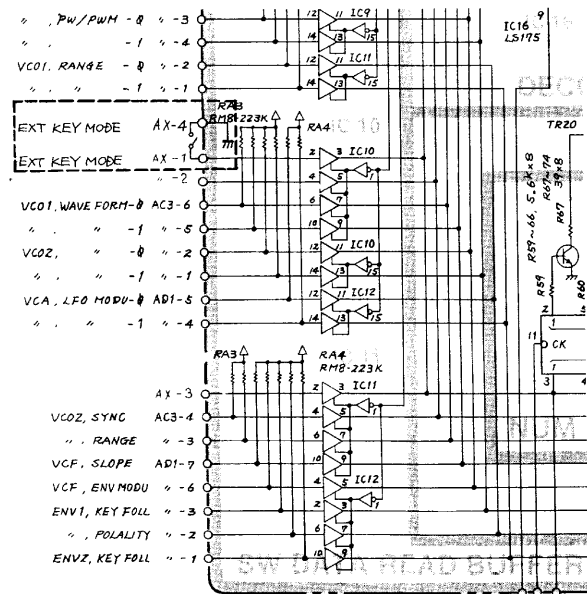
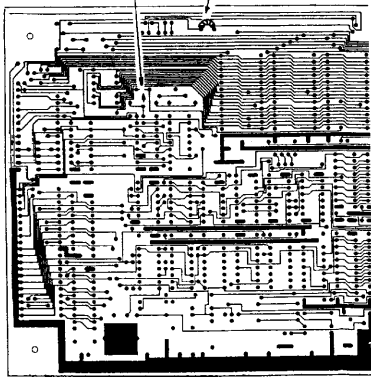
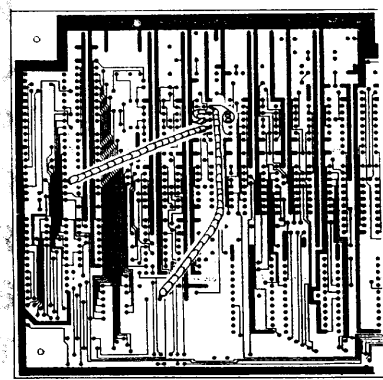
PANEL BOARD A



CPU BOARD



CUT JUMPER



DIAGNOSTIC PROGRAM IN PROM D

On the CPU board (of JP-8 furnished with the OC-8 or DCB board) located is IC33 (3.3D or 3.4D) which contains not only digital communication program, but also diagnostic program. The program, when executed in the TEST mode, simplifies testing and fault isolation of some of the ICs and their associated circuits listing to the right. For this program to run, the remaining PROMs (IC34-IC36) of CPU board must be of 3.2 version.

PRECAUTIONS

Allow plenty of time for warm-up (approx. 30 minutes).
If the CPU, PROMs or other circuits fail to perform their basic functions, the program will not start.

STEPS

1. Turn the JP-8 OFF.
2. To put the JP-8 into the TEST mode, either;
 - a) Turn the power ON while pressing PATCH NUMBER buttons 1 and 3.
 - or
 - b) Set SI-1 and SI-2 of the interface board to TEST, then turn the power ON.

The test program is executed in the order listed and is stopped wherever it encounters a defective IC (or a problem pertaining to a particular IC), and displays the suspected IC number in the window.

To resume the program, press any touch button. (For example, MANUAL.)

At the end of program, the window displays both the PROM D version and the DAC's bit format, for example;

33 12 -- 3.3D, 12-bit DAC
34 14 -- 3.4D, 14-bit DAC

1C 36	IC 3 6	PROM A
1C 35	IC 3 5	PROM B
1C 34	IC 3 4	PROM C
1C 33	IC 3 3	PROM D
1C 06	IC 6	RAM
1C 05	IC 5	RAM
1C 20	IC 2 0	RAM
1C 19	IC 1 9	RAM
1C 04	IC 4	RAM
1C 18	IC 1 8	RAM
DA 00	Module A VCO-1, KCV=0, etc.	
DA 01	IC14, IC15	D/A MSB
DA 02	IC14, IC15	D/A B2
DA 03	IC14, IC15	D/A B3
DA 04	IC14, IC15	D/A B4
DA 05	IC14, IC15	D/A B5
DA 06	IC14, IC15	D/A B6
DA 07	IC14, IC15	D/A B7
DA 08	IC14, IC15	D/A B8
DA 09	IC14, IC15	D/A B9
DA 10	IC14, IC13	D/A B10
DA 11	IC14, IC13	D/A B11
DA 12	IC14, IC13	D/A B12
DA 13	IC14, IC13	D/A B13
DA 14	IC14, IC13	D/A B14

NOTES FOR TABLE

1. 3.3D doesn't check IC5 and IC6.
2. Because of misprogramming, 3.3D will display these IC numbers in reverse order. If displayed, read; IC20 as IC19, and IC19 as IC20.
3. Output from Module A VCO-1 is applied to the DAC Check. Consequently, if this VCO fails, all the remaining tests will not be performed.
Push any button, and the version with 00 is displayed.
4. IC13 and IC15 on the 12-bit interface board are inversely numbered.
Read; IC13 as IC15, and IC15 as IC13.
5. If the 13-bit line malfunctions in the 14-bit D/A, the CPU concludes that the D/A is 12-bit, and skips the 13th and 14th bits.

DESCRIPTION OF CONNECTION CABLES

In the below, SN refers to Serial Number of OP-8.

• For serial numbers up to and including SN220269, the OP-8 was provided with Flat Cable H146 for connecting the OP-8 to the JP-8.

• Effective from serial number SN230270, the OP-8 unit can be connected to the JP-8 through the Flat Cable H146 provided with the OC-8 unit, or to the JUNO-60 through the DCB Cable H165 provided with the OP-8 unit.

• Roland provides not only DCB Cable H165 but also DCB Cable H172 for interconnecting JP-8 or JUNO-60 as shown here.

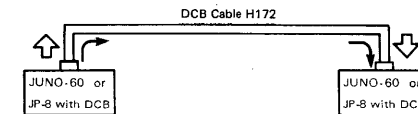
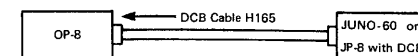
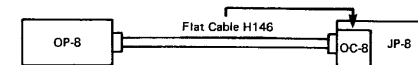
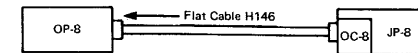
• DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.

When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.

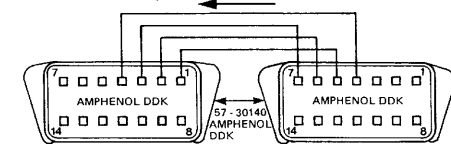
Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.

Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.

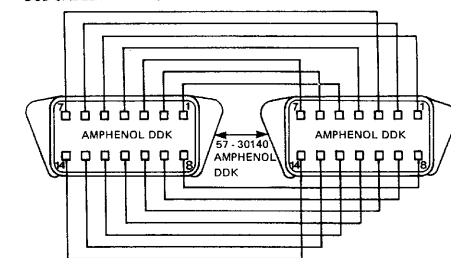
On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.



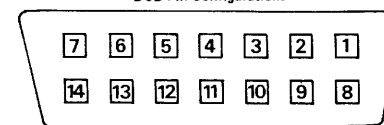
DCB CABLE H172 (Length: 3m)



DCB CABLE H165 (Length: 1.5m)



DCB Pin Configurations



(View from Rear Panel)

- | | | |
|----------|------|---------------|
| 1. BUSY |) RX | 8. UNREG |
| 2. DATA | | 9. VCA LOWER |
| 3. CLOCK | | 10. VCA UPPER |
| 4. GND | | 11. VCF LOWER |
| 5. BUSY |) TX | 12. VCF UPPER |
| 6. DATA | | 13. VCO-2 |
| 7. CLOCK | | 14. VCO-1 |

APPENDIX

PCB EDITION

Dot and circle above PCB code are indicative of edition; "●" stands for 1, and "○" for 5. Example: ○● = 6th edition.

Illustrated on pp. 48-50 is information on MODULE and MODULE CONTROLLER Boards mounted on the JP-8 models with serial numbers up to 090599. For circuit diagram, refer to p.11 or p.12 although some small discrepancies may exist.

CAUTION ON REPLACEMENT OF PCBs IN THIS SECTION

Although terminal for terminal compatible, when mix used, new and old PCBs process signals in slightly different way, reproducing voices that are distinguishable from each other. Therefore, when replacing MODULE or MOD CON board in this section, use a set of PCBs of the same edition group as described below.

NOTE: Replacement of MODULE board can be made independently of MOD CON board, and vice versa.

MODULE CONTROLLER BOARD group A	MODULE BOARD group B	When replacements for MOD CON are of group B, check IC49 (RAM) for name. If it is 5101, see p.38 for necessary modification.
○●2H269 or ○●52H269	○●52H269-up ○●52H270-up	

Listing below are descriptions of surface mounting, jumper wire, and conductive foil cut made on the MOD COM boards up to the abovementioned serial numbers, shown on the next page.

ABBREVIATIONS

C-pattern cut Di-diode R-resistor J-jumper M-mylar cap

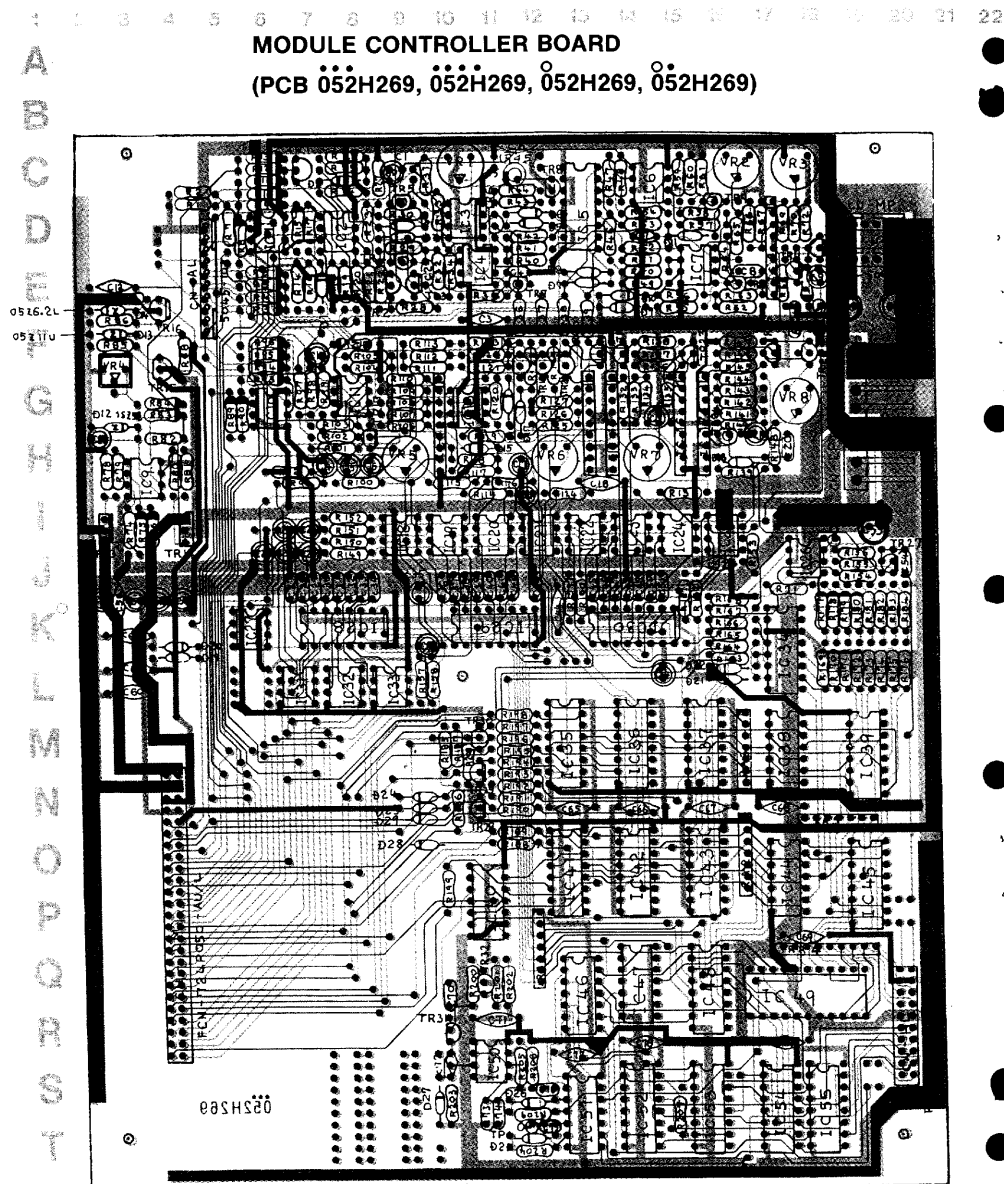
Serial numbers

1B-050199 2A-050200 2B-060299 3A-060300 4A-070400 5A-080500 5B-090599

No.	Part	SN	No.	Part	SN
1	C	up to 2B	10	R	5A-up
2	C	3A-5B	11	R	3A-5B
3	C				
4	D	up to 1B	12	D 2xC	3A-5B
5	R	3A-5B	13	M.R.C	2A-up
6	J	up to 2B	14	J.C	4A-5B
7	J.C	4A-5B	15	M	4A-5B
8	J	5A-up	16	J.C	2A-5B
9	R	up to 2B	17	M	3A-5B

MODULE CONTROLLER BOARD

(PCB ○●2H269, ○●52H269, ○●52H269, ○●52H269)



PARTS LIST CHANGE

PART. SERIAL NO.	FROM	TO	PART NO.
INTERFACE BOARD			
SN 171700 PCB Ass'y PCB D/A Converter (IC14) Latches	OPH122 052H268 Am6012 LS273 LS175 LS175 TC4051	OPH122A 052H268 ITS80141 TC40H273 (IC15, CMOS) TC40H174 (IC13, CMOS) TC40H175 (IC11, CMOS) HD 14051 (CMOS) (Hitachi only) TC4001 4013BP (CMOS)	149H122A 15219127 15159507 15159511 15159512 15159113H0
IC25, IC26	TC4051	HD 14051 (CMOS) (Hitachi only)	15159113H0
IC22 IC9	LS02 74LS74	TC4001 4013BP (CMOS)	15159101T0 15159105T1
SN 212330 IC9	4013	TC40H74P	15159510
	ICs: ALL INCOMPATIBLE		

CPU BOARD

SN 171700 IC34-IC36	μPD2716 (version 1.0)	μPD2716-JP8-A (IC36) μPD2716-JP8-B (IC35) μPD2716-JP8-C (IC34)	15179609 (version 3.x) 15179610 (version 3.x) 15179611 (version 3.x) (version 3.x = 3.1 or 3.2)
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MODULE CONTROLLER BOARD

SN 202100 PCB Ass'y PCB IC3 Ladder Resistor TRs, 11, 12, 25 TR26 Switches	OPH123 052H269 TL082 Discrete 2SA1015 2SC1815	OPH123A 052H269 BA662A R601611 (RA6) 2SA798-G (TR11) 2SA798-G (TR25) SSB212 (SWs 1, 2)	149H123A 15229802 15119108 15119108 13159123
SN 202210 IC49 RAM	2101 only (Compatible with minor modification. See pp. 37, 38.)	2101 or 5101	15179303

PANEL BOARD F

LED (display) SN 242750	LN526RA	LN5260A	15029409
	(Compatible but different in brightness and color; mix use should be avoided.)		

PANEL BOARD E PANEL BOARD G

SN 272850 Switches (LEDs)	KHC11901 (AR3432S)	KHC11026 (SEL2210R)	13169610
	(Switch proper remains unchanged. The new LED has better off-axis luminous density. Mix use should be avoided.)		

SN 282880-UP JP-8 WITH DCB BOARD

PART NAME	FROM	TO	PART NO.
Top Panel Chassis (jack) Holder (rear)	Panel H78B Chassis H116	Panel H78C Chassis H116A Holder H184	072H078C 061H116A 064H184

DCB BOARD

PCB Ass'y Holder IC1 IC3 Flat Cable Flat Cable H126 (INTFACE-CPU)	OPH220 Holder H185 74LS21 μPD8251AC Flat Cable H213 (INTERFACE-CPU-DCB)	149H220 (pcb 052H380B) 064H185 15169350 15179112 053H213
DCB Connector Holder Slide Switch	57-40140R Holder H153 SSB-022-12RN	13429611 064H153 13159118

CPU BOARD

IC33	μPD2716-JP8-D	15179612 (version 3.4)
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In order to expedite delivery of products or because of procurment problem, the factory is occasionally forced to make minor substitution of ICs. Such substitutions will work satisfactorily and compatible with the initial IC unless otherwise noted in related sections (circuit diagram, parts list, etc.).

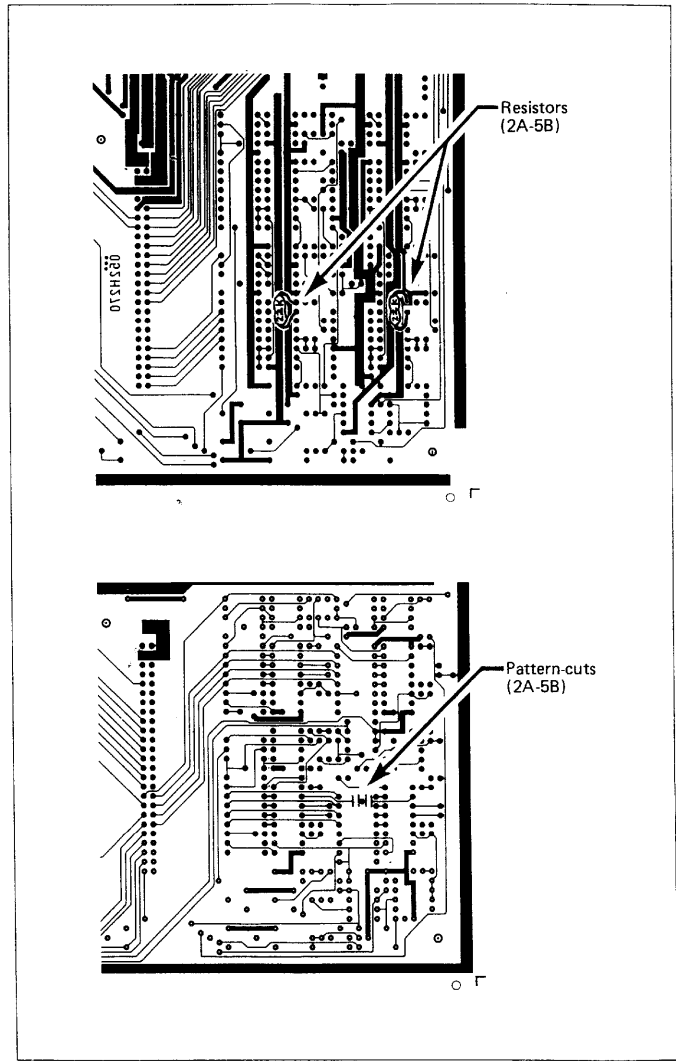
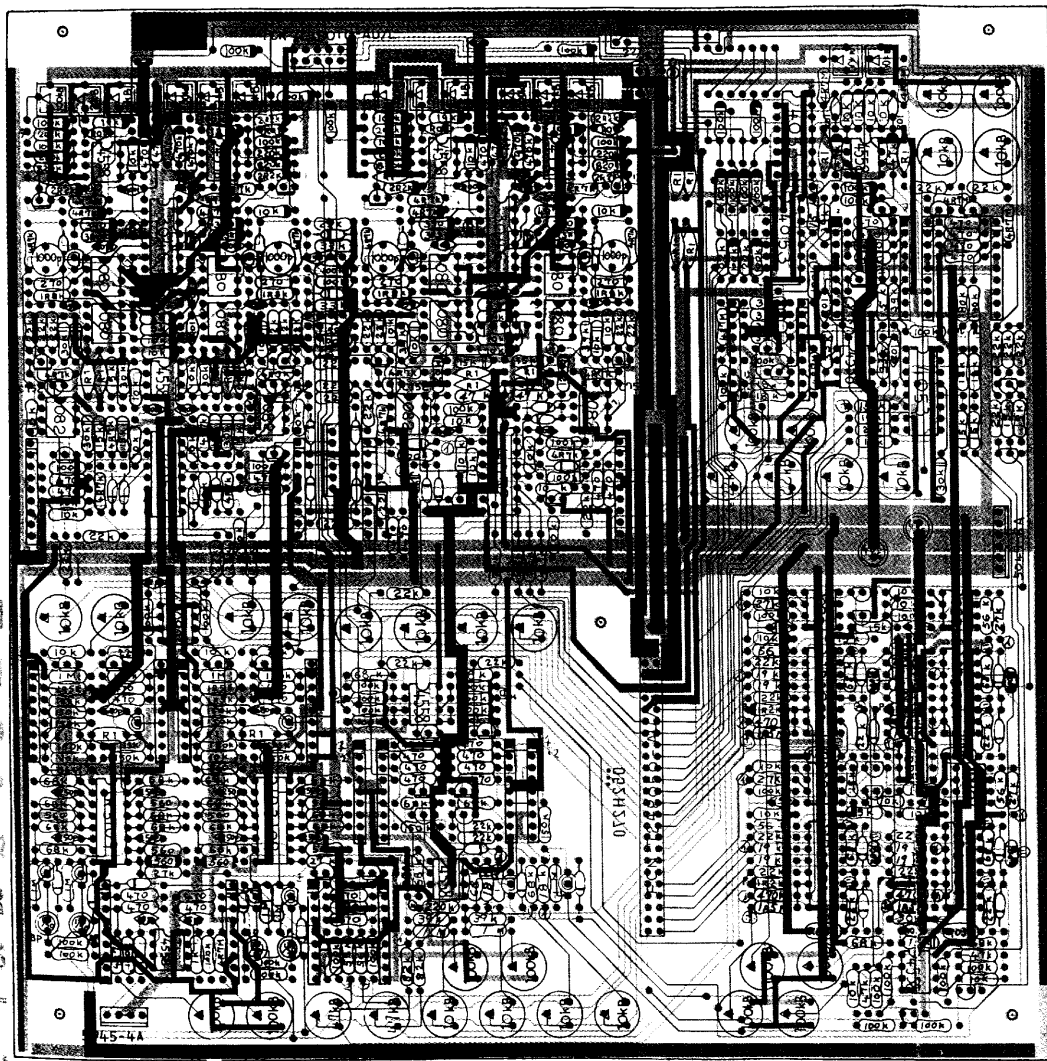
PART NUMBER

Usually, equivalent semiconductors are assigned to the same part number as initial component with two-letter suffix identifying the manufacturer. For example, TO - Toshiba, ZO - Motorola. In ordering such ICs, uncertain suffix can be omitted from the part number, and the factory will supply suitable ones with notes or cautions, as necessary.

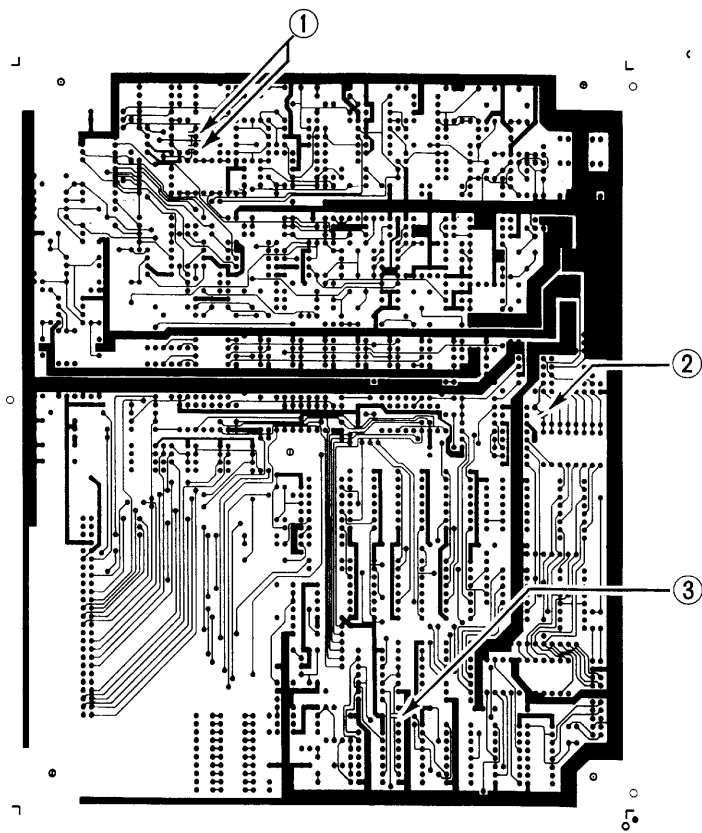
Parts on the PARTS LIST	Equivalent
TC4052BP	HD 14052BP
TC4051BP	HD 14051BP
TC40175BP	μPD4175BC
μPD2101ALC	M5L2101AP-4 μPD5101LC M5L5101LP-1
μPD780C-1	LH0080A
μPD2716D	M5L2716K MB8516
μPD444C	M58981P-45
μPD2114C	M5L2114LP
μPD8253C	M5L8253P-5
TL082CP	NJM082DR μPC4082C
74LS Series	M74LS series
74... Series (exp. 7406)	M532... series M53206)

MODULE BOARD OPH124

SN 030100-090599 (pcb 052H270 or 052H270)



PATTERN-CUTS ON MOD CON



PATTERN-CUTS & SURFACE-MOUNTINGS ON MOD CON

